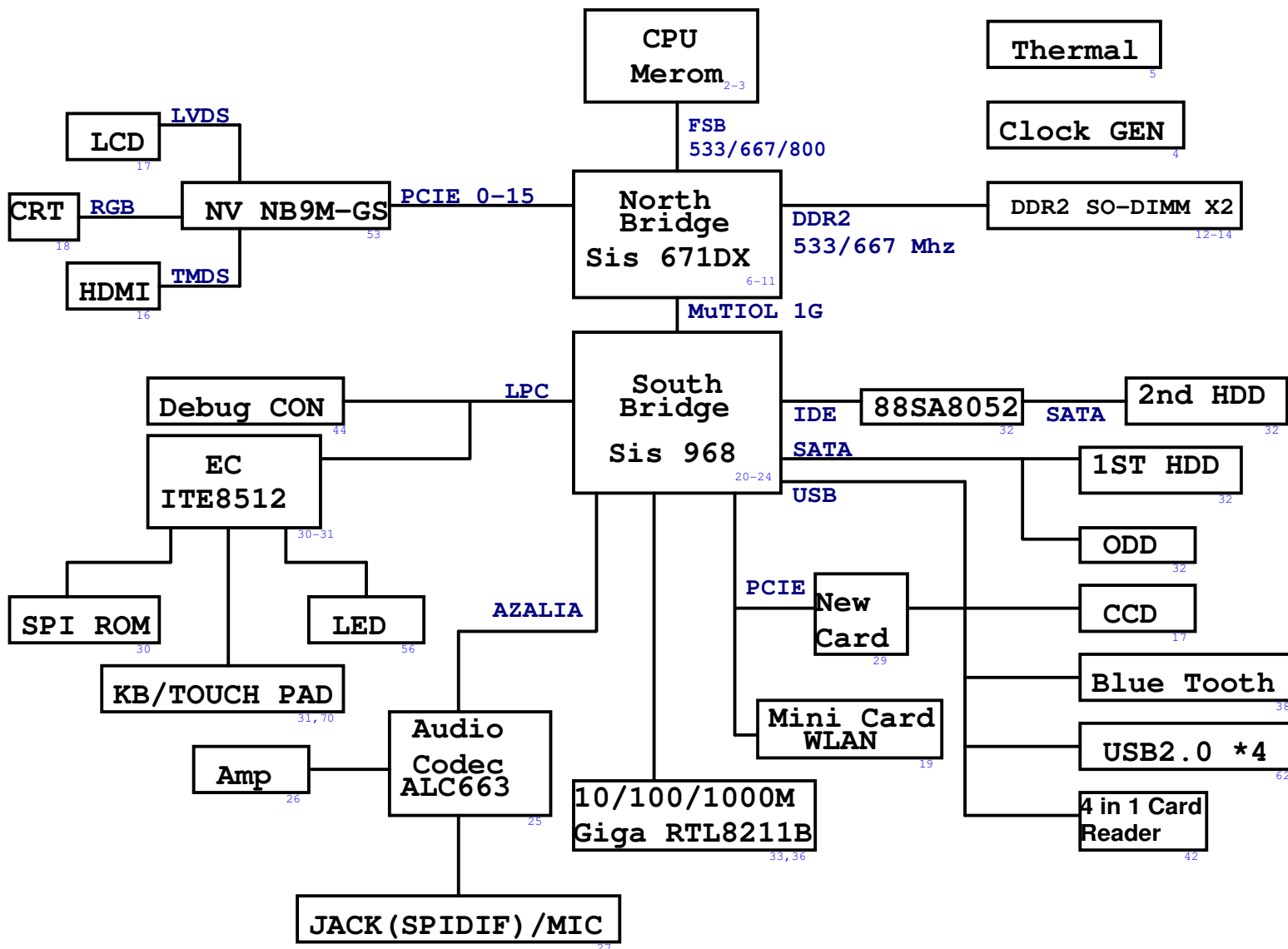


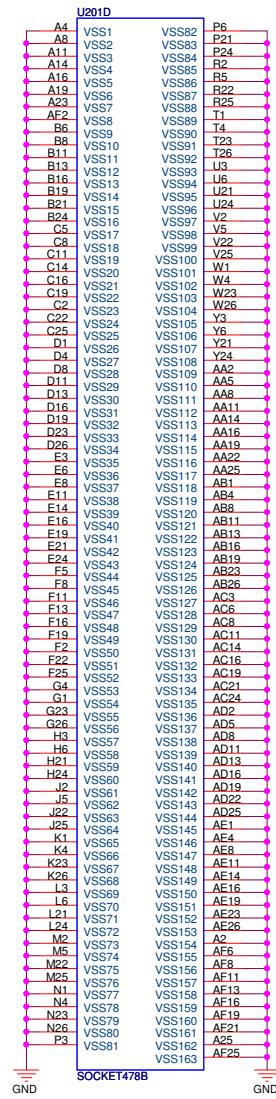
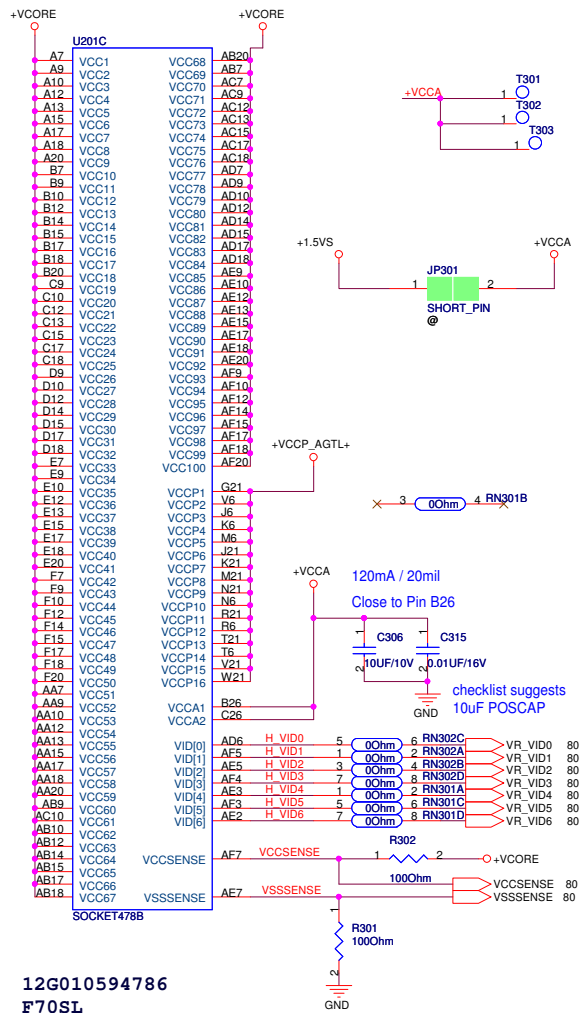
# F70SL Main BD. R1.0 BLOCK DIAGRAM





YUNAH FSB667	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
C4	C3	C0	
ICC	0.9A	7.59A	27A

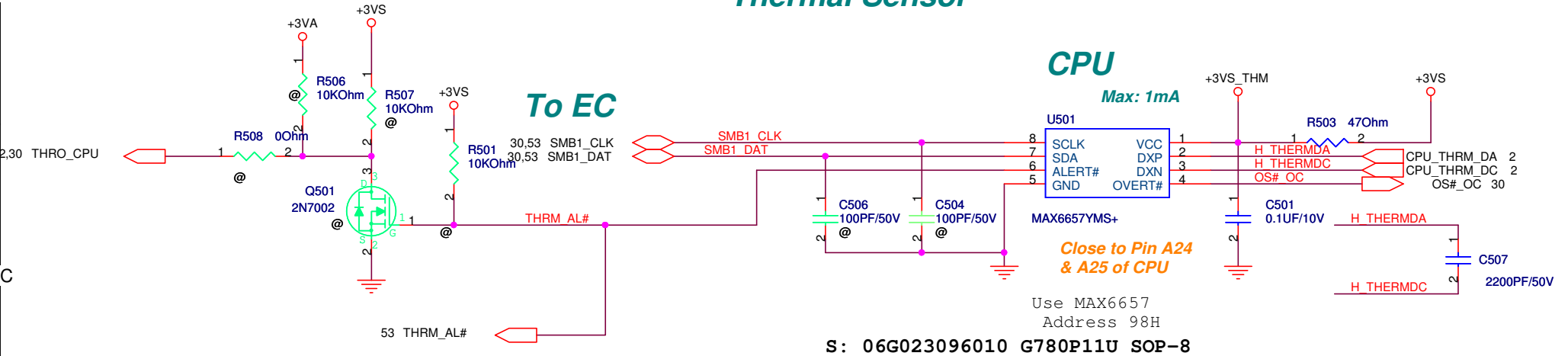
YUNAH FSB667	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
Min	Typ	Max	
ICCP			2.5A



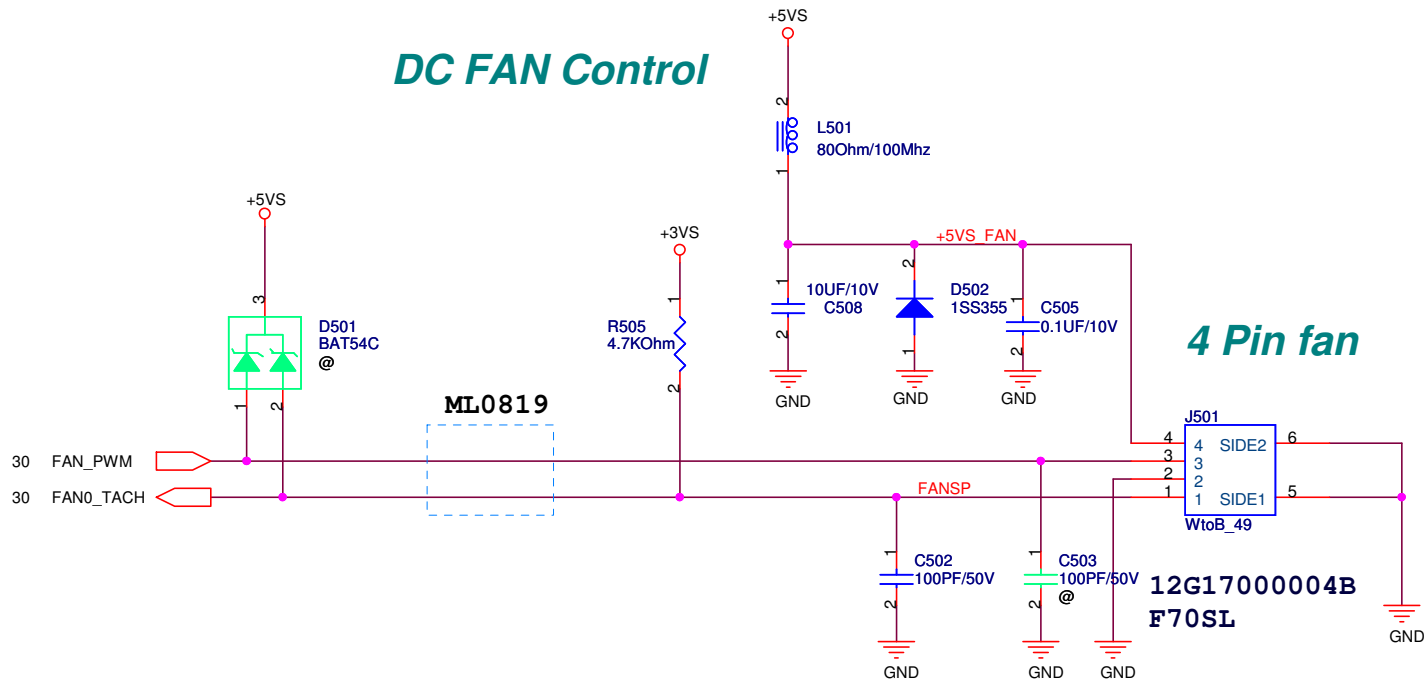
Layout Note:  
VCCSENSE/VSSSENSE lines between the CPU and the VR should have a trace width of 18 mils on 7 mils spacing, with trace impedance of  $Z_0=27.4 \text{ Ohm}$ .  
The VCCSENSE/VSSSENSE should be length matched to within 25 mils.  
These resistors should be placed within 2 inch of the CPU.



## Thermal Sensor



## DC FAN Control



Route H\_THERMDA and H\_THERMDC on the same layer

-----OTHER SIGNALS

20 mils

=====GND

10 mils

=====H\_THERMDA(10 mils)

10 mils

=====H\_THERMDC(10 mils)

10 mils

=====GND

20 mils

-----OTHER SIGNALS

Avoid FSB,Power

<b>ASUS</b>		<b>Title : Thermal Sensor</b>	
ASUSTeK Computer INC		Engineer: Miller / Daniel	
Size A4	Project Name <b>F70SL</b>		Rev 1.0
Date: Monday, November 03, 2008		Sheet 5	of 94

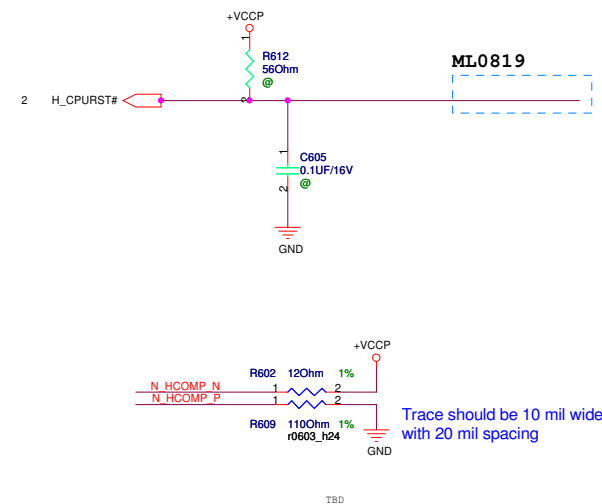
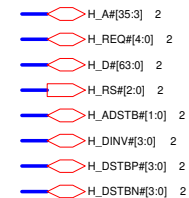
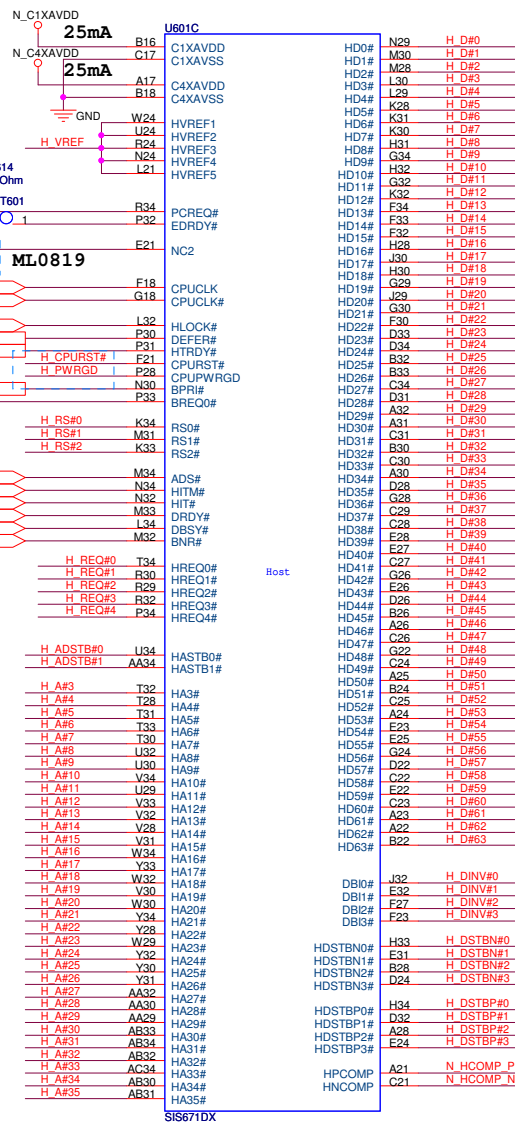
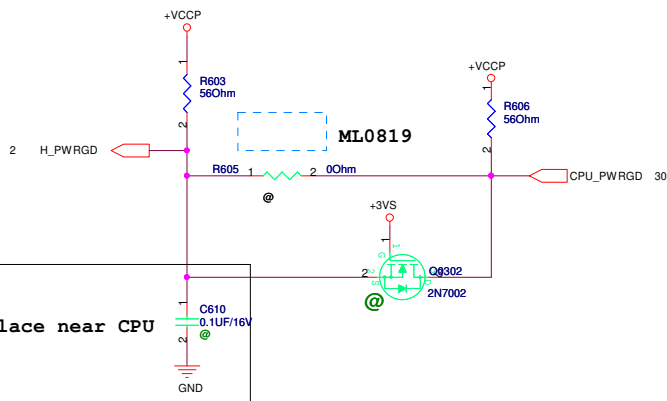
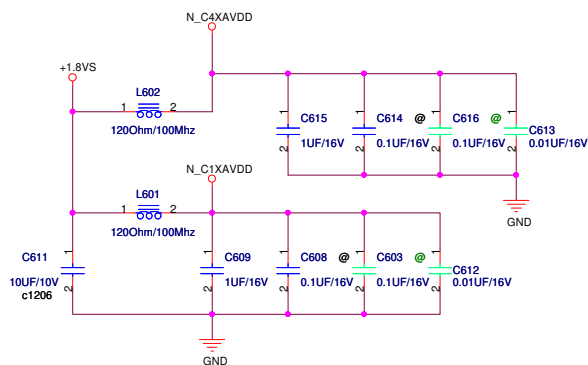
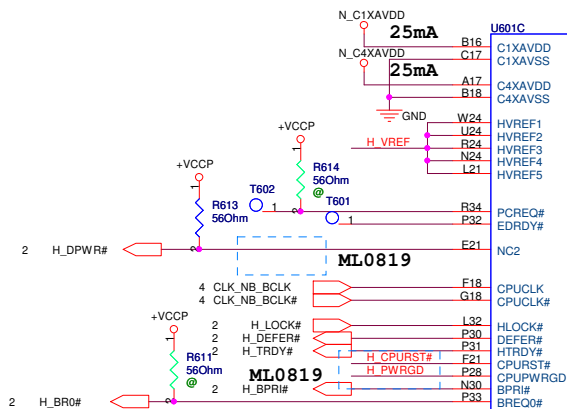
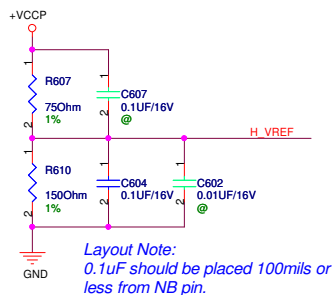
5

4

3

2

1

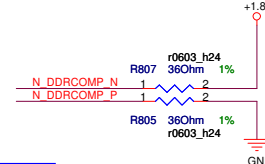
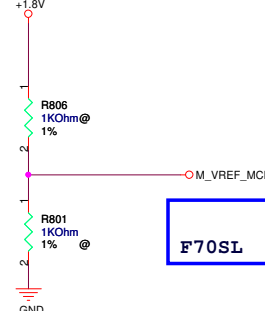
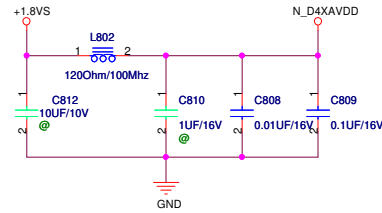
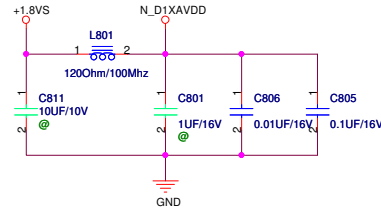
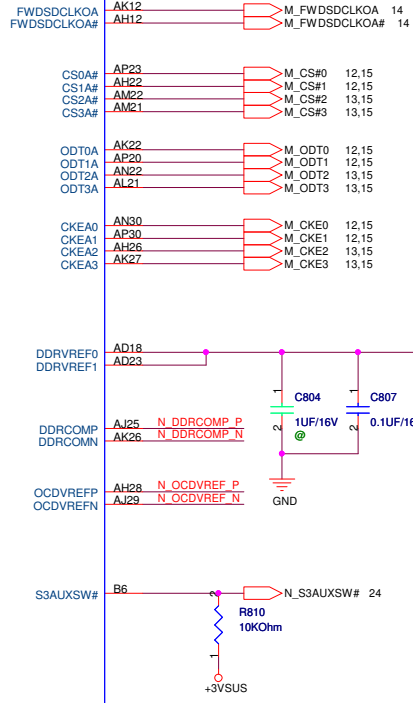


<b>ASUS</b>		<b>Title : M671DX (HOST)</b>	
ASUSTek Computer INC		Engineer: Miller / Daniel	
Size A3	Project Name <b>F70SL</b>	Rev 1.0	
Date: Monday, November 03, 2008	Sheet 6	of 94	



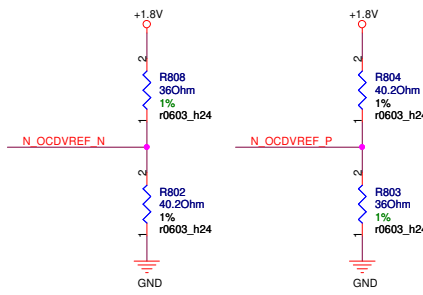
U601B		
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M_A_DQ1	AD30	MD1A
M_A_DQ2	AG34	MD2A
M_A_DQ3	AE29	MD3A
M_A_DQ4	AF32	MD4A
M_A_DQ5	AF34	MD5A
M_A_DQ6	AF31	MD6A
M_A_DQ7	AE30	MD7A
M_A_DM0	AD28	DQM0A
M_A_DQS0	AF32	DQS0A
M_A_DQS#0	AF33	DQS0A#
M_A_DQ8	AF28	MD8A
M_A_DQ9	AJ34	MD9A
M_A_DQ10	AH31	MD10A
M_A_DQ11	AG30	MD11A
M_A_DQ12	AF30	MD12A
M_A_DQ13	AG32	MD13A
M_A_DQ14	AJ32	MD14A
M_A_DQ15	AJ31	MD15A
M_A_DM1	AH34	DQM1A
M_A_DQS1	AH32	DQS1A
M_A_DQS#1	AH33	DQS1A#
M_A_DQ16	AK34	MD16A
M_A_DQ17	AH30	MD17A
M_A_DQ18	AL32	MD18A
M_A_DQ19	AM33	MD19A
M_A_DQ20	AK32	MD20A
M_A_DQ21	AG29	MD21A
M_A_DQ22	AM34	MD22A
M_A_DQ23	AL31	MD23A
M_A_DM2	AJ30	DQM2A
M_A_DQS2	AK33	DQS2A
M_A_DQS#2	AL34	DQS2A#
M_A_DQ24	AM32	MD24A
M_A_DQ25	AP32	MD25A
M_A_DQ26	AP31	MD26A
M_A_DQ27	AM29	MD27A
M_A_DQ28	AK30	MD28A
M_A_DQ29	AK29	MD29A
M_A_DQ30	AJ27	MD30A
M_A_DQ31	AK28	MD31A
M_A_DM3	AN32	DQM3A
M_A_DQS3	AM30	DQS3A
M_A_DQS#3	AM31	DQS3A#
M_A_DQ32	AK20	MD32A
M_A_DQ33	AM20	MD33A
M_A_DQ34	AM19	MD34A
M_A_DQ35	AJ19	MD35A
M_A_DQ36	AJ20	MD36A
M_A_DQ37	AJ21	MD37A
M_A_DQ38	AP19	MD38A
M_A_DQ39	AH20	MD39A
M_A_DM4	AK21	DQM4A
M_A_DQS4	AK19	DQS4A
M_A_DQS#4	AL19	DQS4A#
M_A_DQ40	AK18	MD40A
M_A_DQ41	AJ17	MD41A
M_A_DQ42	AK17	MD42A
M_A_DQ43	AP16	MD43A
M_A_DQ44	AH18	MD44A
M_A_DQ45	AP18	MD45A
M_A_DQ46	AP17	MD46A
M_A_DM5	AM18	MD47A
M_A_DQS5	AL17	DQM5A
M_A_DQS#5	AM17	DQS5A
M_A_DQ48	AN16	MD48A
M_A_DQ49	AK16	MD49A
M_A_DQ50	AN14	MD50A
M_A_DQ51	AJ15	MD51A
M_A_DQ52	AP15	MD52A
M_A_DQ53	AM16	MD53A
M_A_DQ54	AK15	MD54A
M_A_DQ55	AP14	MD55A
M_A_DM6	AH16	DQM6A
M_A_DQS6	AL15	DQS6A
M_A_DQS#6	AM15	DQS6A#
M_A_DQ56	AL13	MD56A
M_A_DQ57	AM13	MD57A
M_A_DQ58	AM12	MD58A
M_A_DQ59	AJ13	MD59A
M_A_DQ60	AM14	MD60A
M_A_DQ61	AK14	MD61A
M_A_DQ62	AH14	MD62A
M_A_DM7	AK13	DQM7A
M_A_DQS7	AP12	DQS7A
M_A_DQS#7	AP13	DQS7A#

DRAM



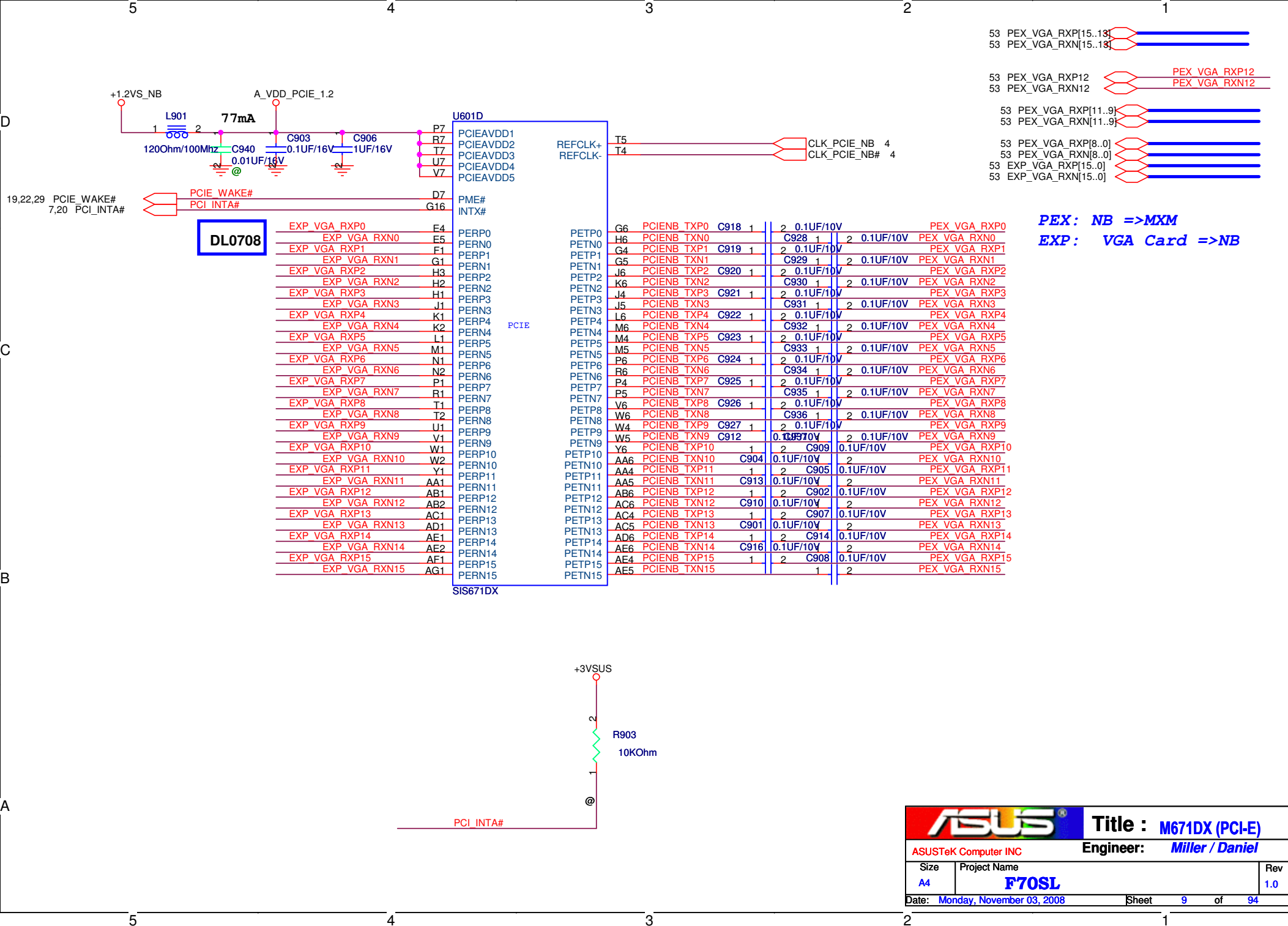
F70SL  
DL0623

Layout Note:  
Route as  
short as  
possible



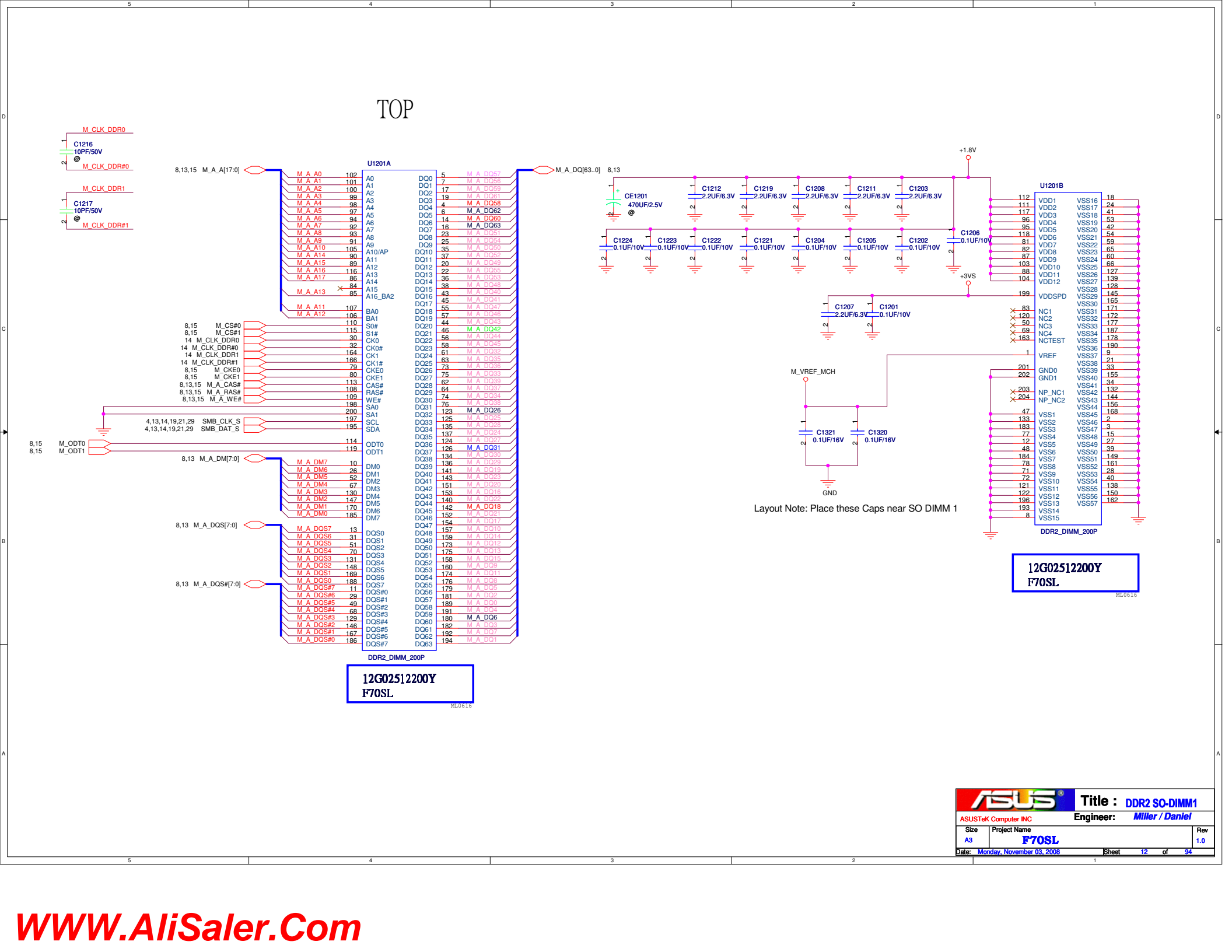
ASUS		Title : M671DX (DDR2)	
ASUSTek Computer INC		Engineer: Miller / Daniel	
Size A3	Project Name F70SL	Rev 1.0	
Date: Monday, November 03, 2008		Sheet 8	of 94









[illegible][illegible]

TOP

12G02512200Y F70SL

12G02512200Y F70SL

Layout Note: Place these Caps near SO DIMM 1

12G02512200Y F70SL

ASUS  
ASUSTek Computer INC  
Title : DDR2 SO-DIMM1  
Engineer: Miller / Daniel  
Size Project Name  
AS F70SL  
Date: Monday, November 03, 2008 Sheet 12 of 94 Rev 1.0

TOP

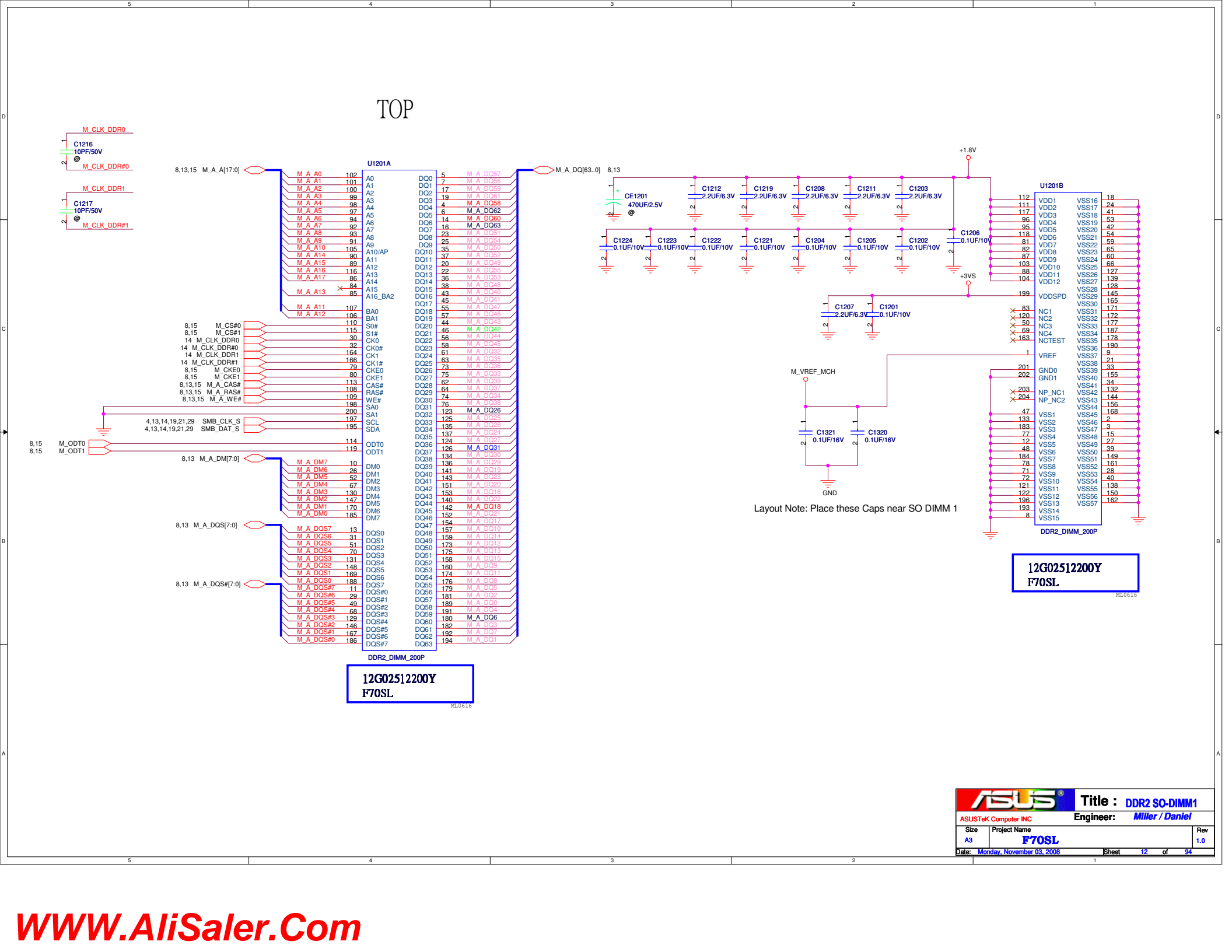
12G02512200Y F70SL

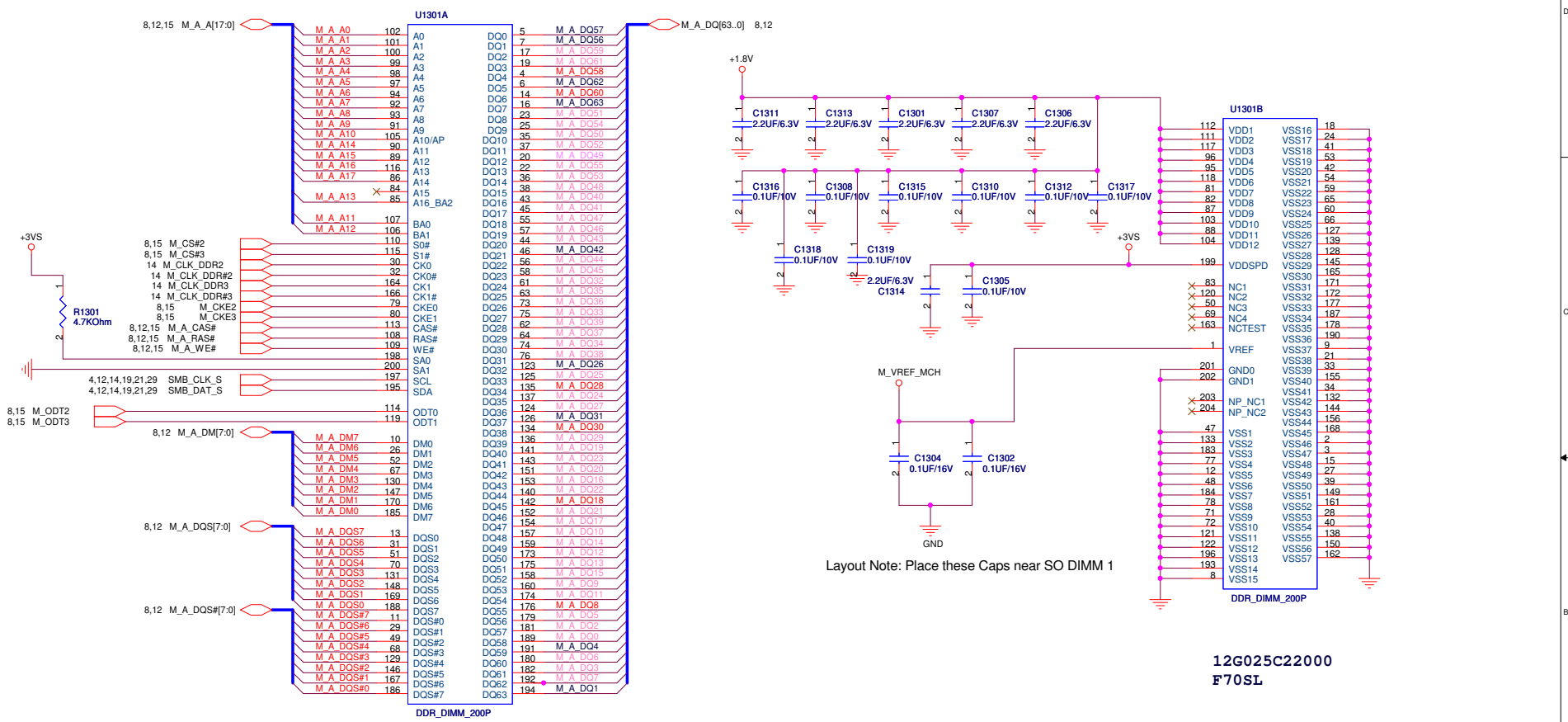
12G02512200Y F70SL

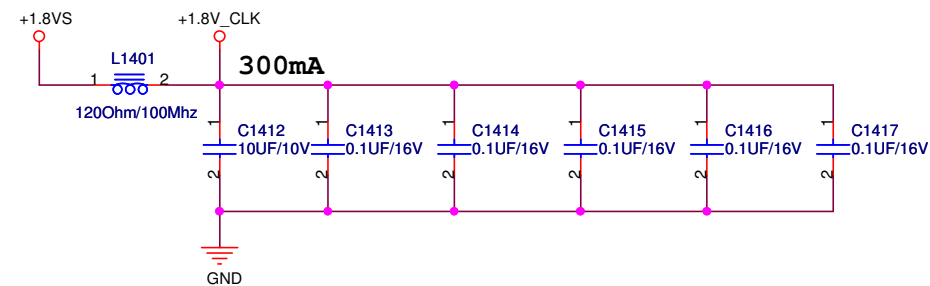
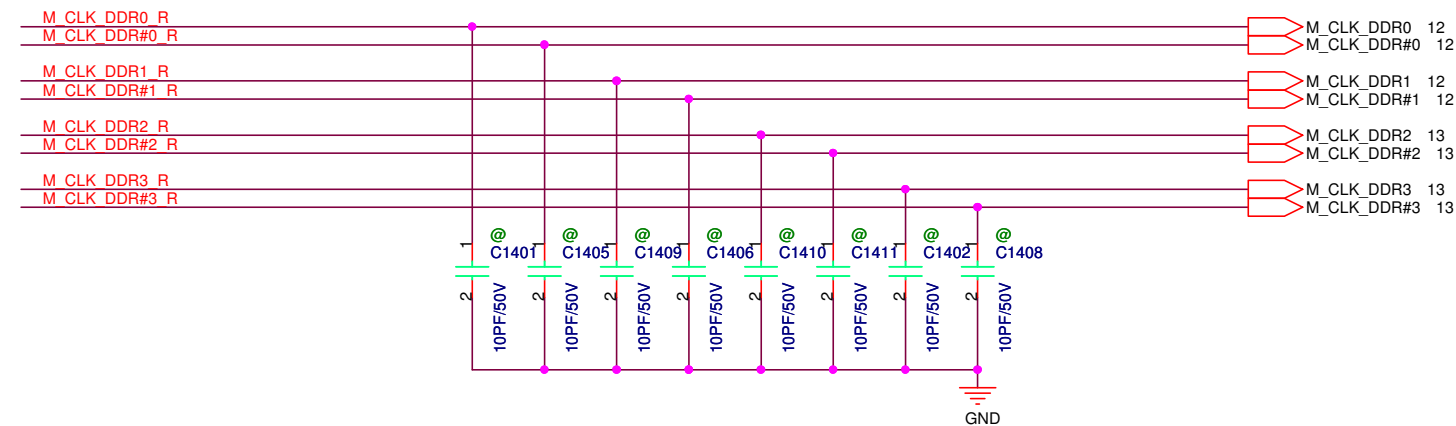
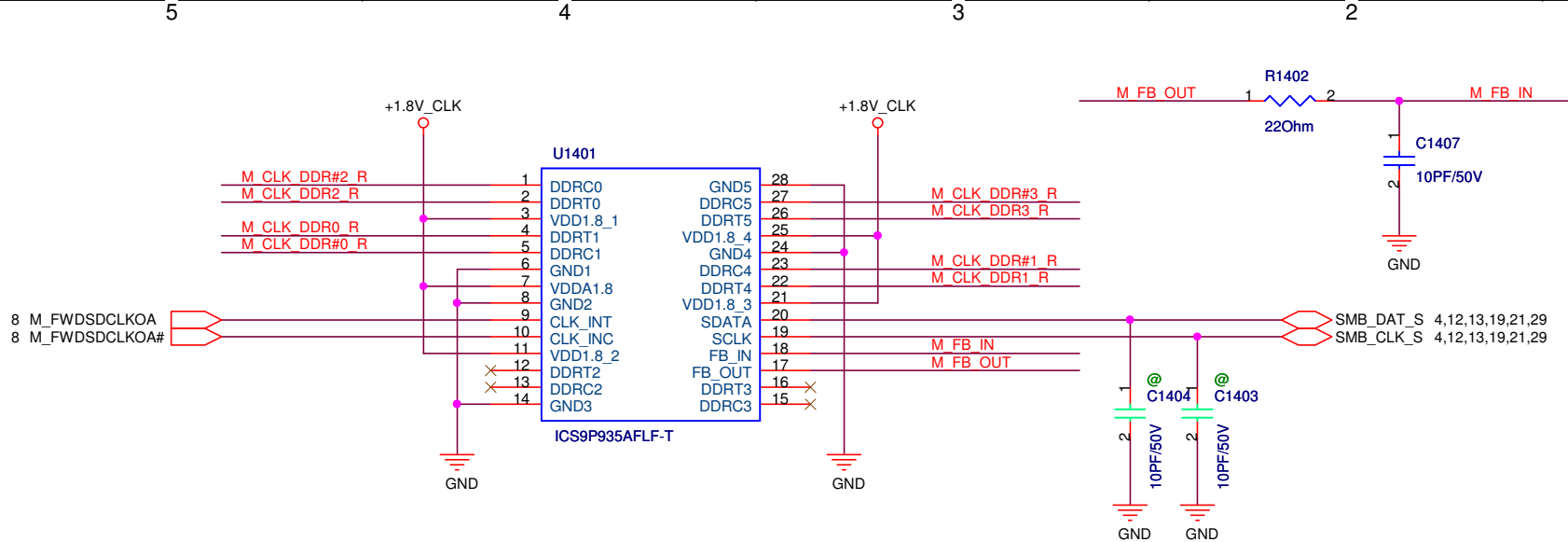
Layout Note: Place these Caps near SO DIMM 1

12G02512200Y F70SL

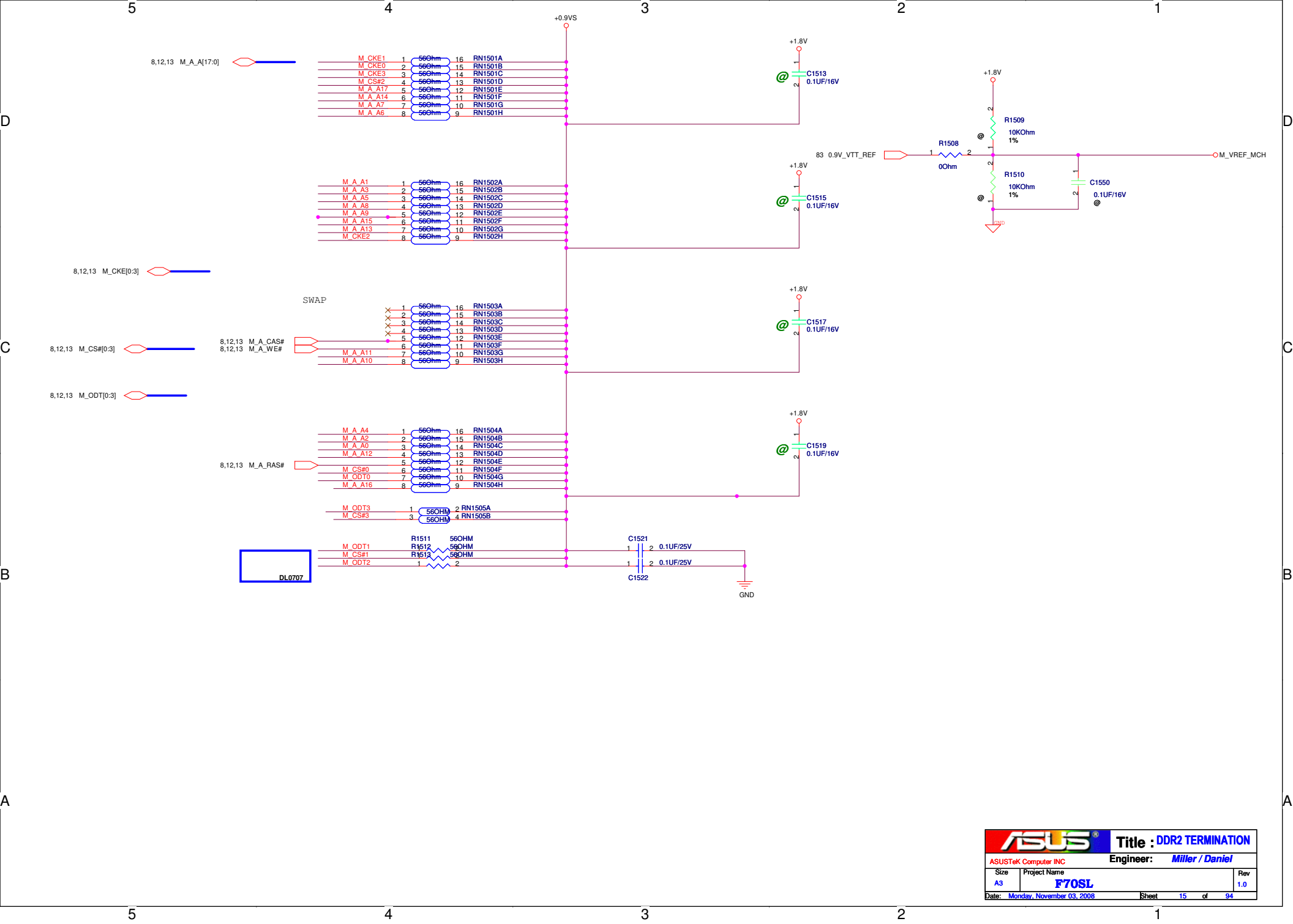
ASUS  
ASUSTek Computer INC  
Title : DDR2 SO-DIMM1  
Engineer: Miller / Daniel  
Size Project Name  
AS F70SL  
Date: Monday, November 03, 2008 Sheet 12 of 94 Rev 1.0

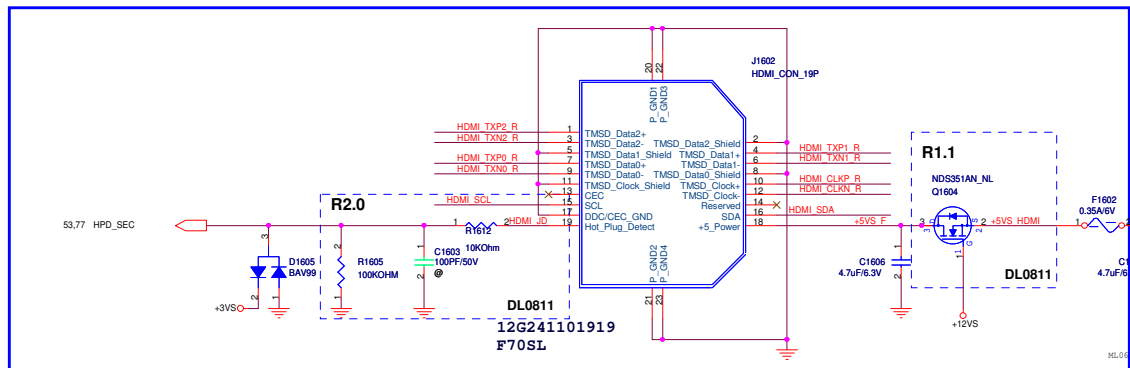
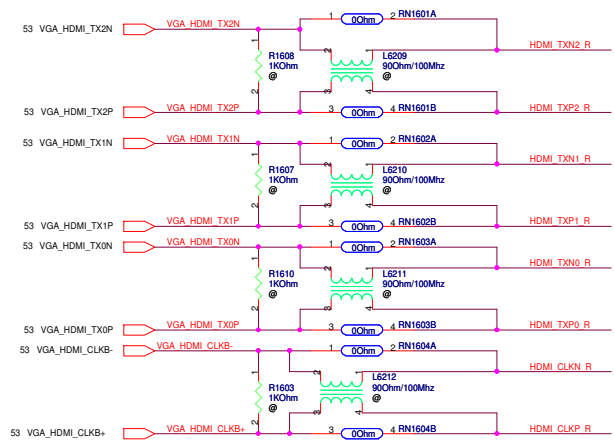
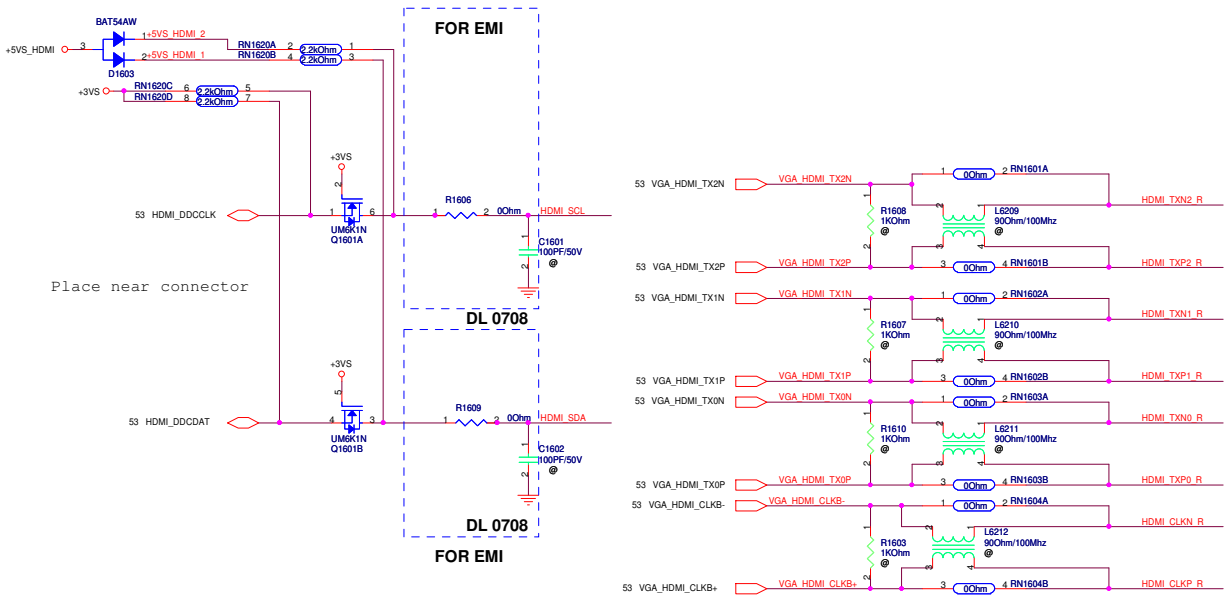






<b>ASUS</b>		<b>Title : DDR2 BUFFER</b>	
ASUSTeK Computer INC		Engineer: <b>Miller / Daniel</b>	
Size <b>A4</b>	Project Name <b>F70SL</b>		Rev <b>1.0</b>
Date: <b>Monday, November 03, 2008</b>		Sheet <b>14</b> of <b>94</b>	



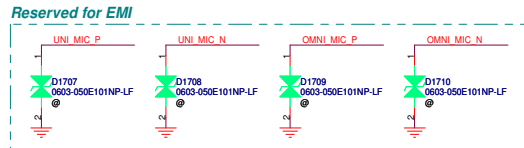




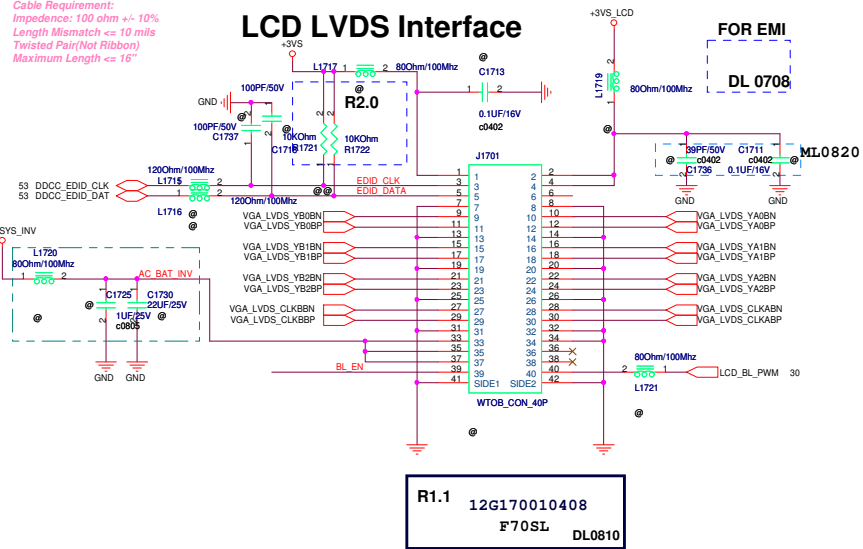
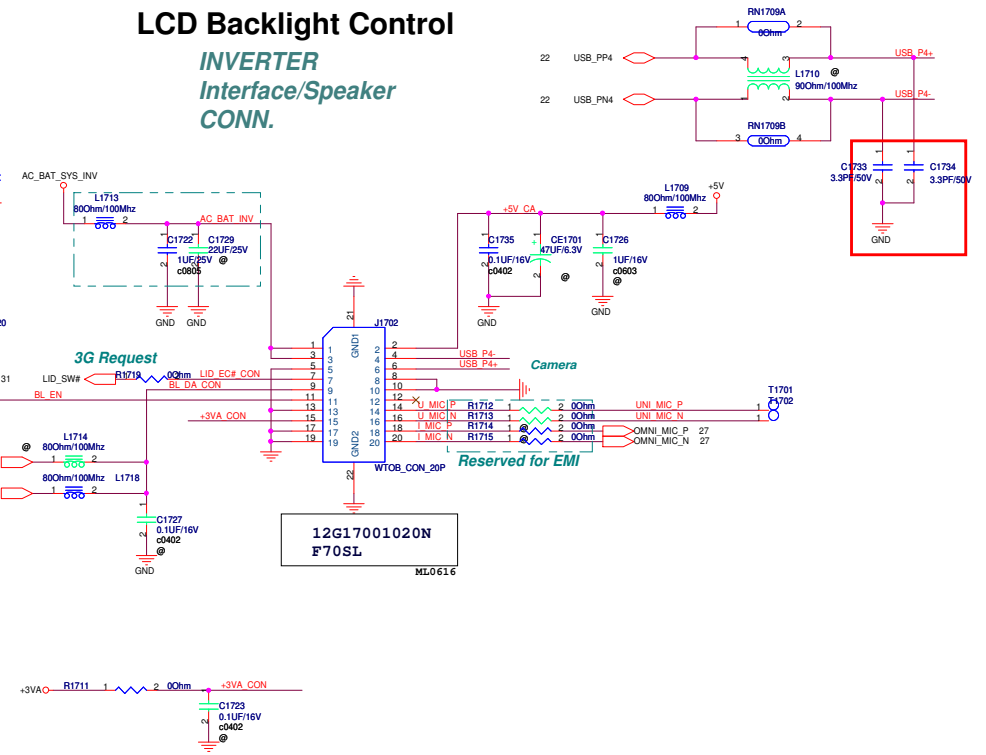
## SI3865: US\$0.22

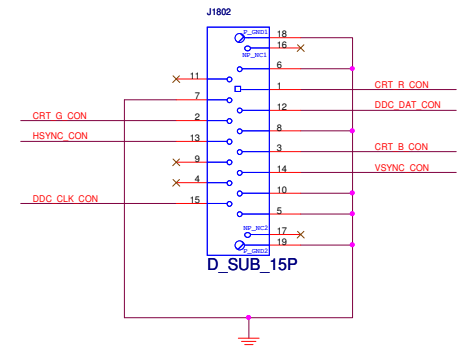


## B to B Interface



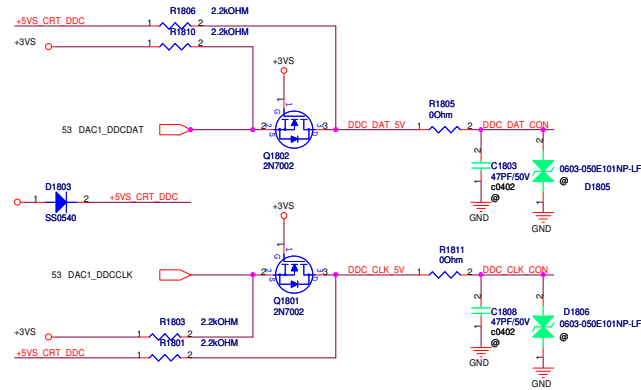
+3VS

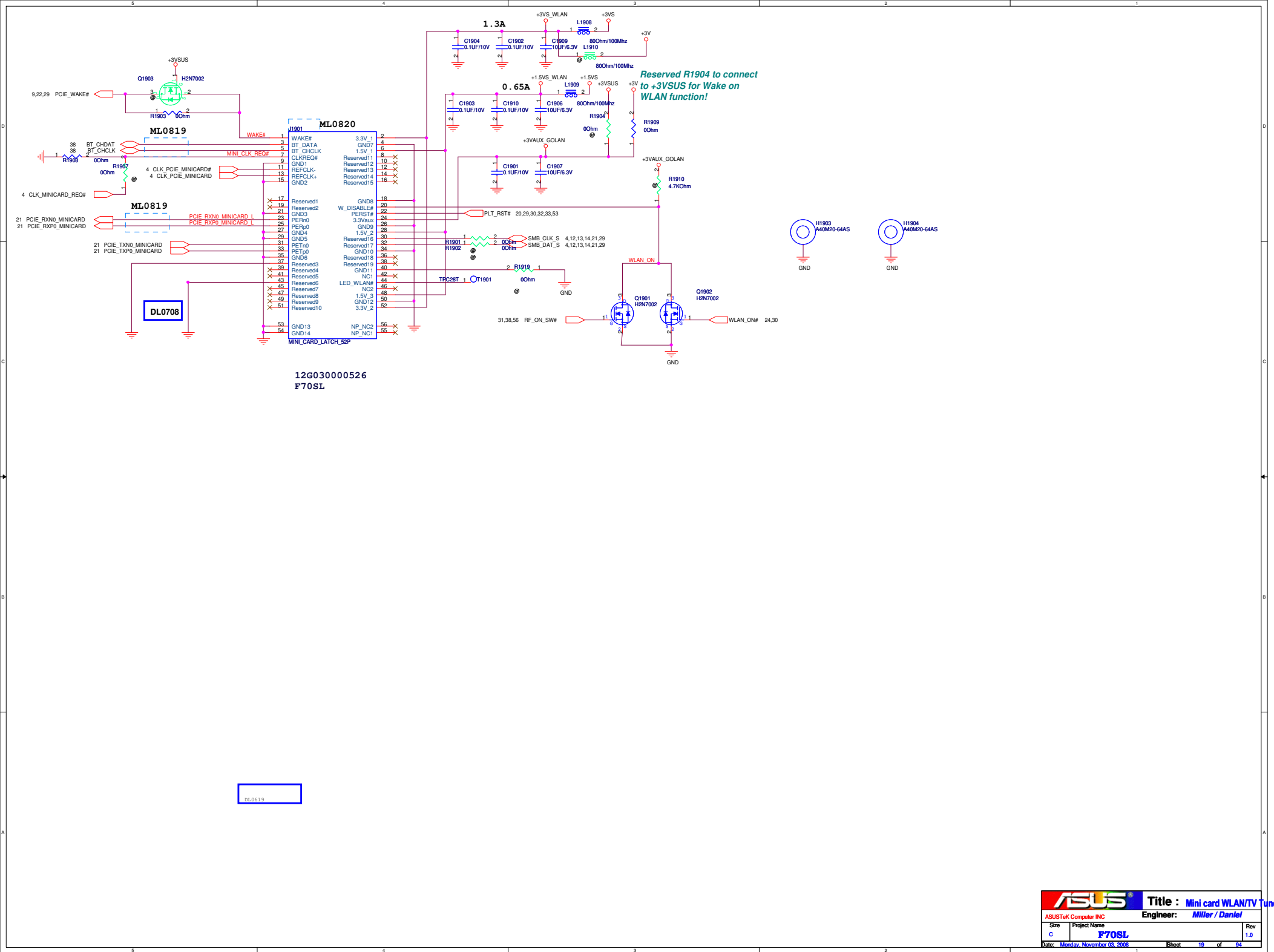
**INVERTER**  
**Interface/Speaker**  
**CONN.**

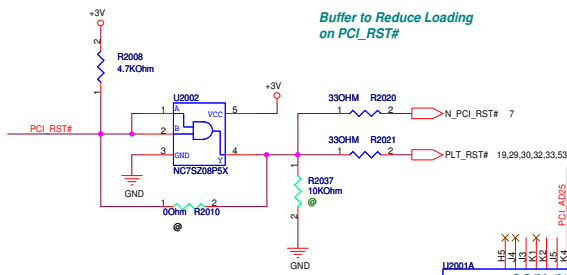


Close to the CRT Connector

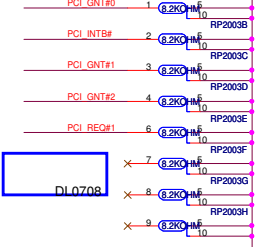
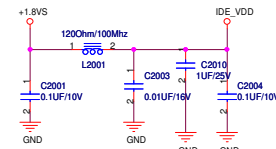
```
06G004600811
F70SL  cost down: 0.28
DL0702
```



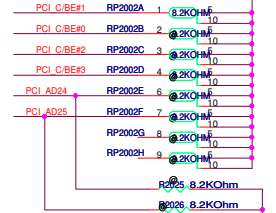




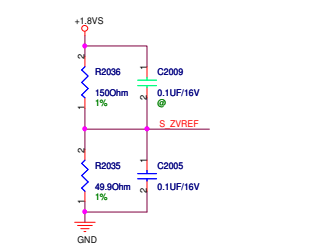
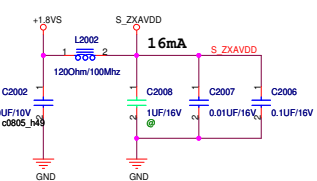
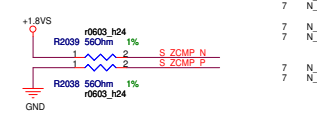
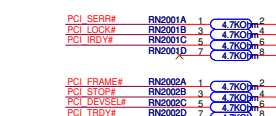
DL0626



DL0708



DL0630



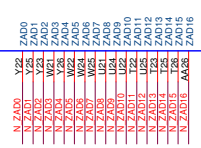
PCI

IDE

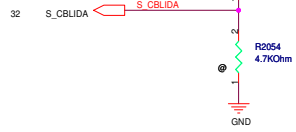
MuTIOL

SPI

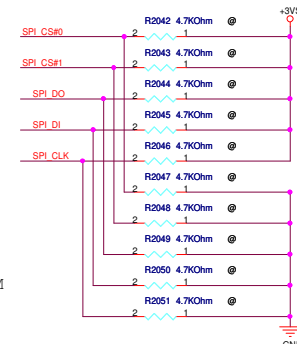
P/N 02G020003910

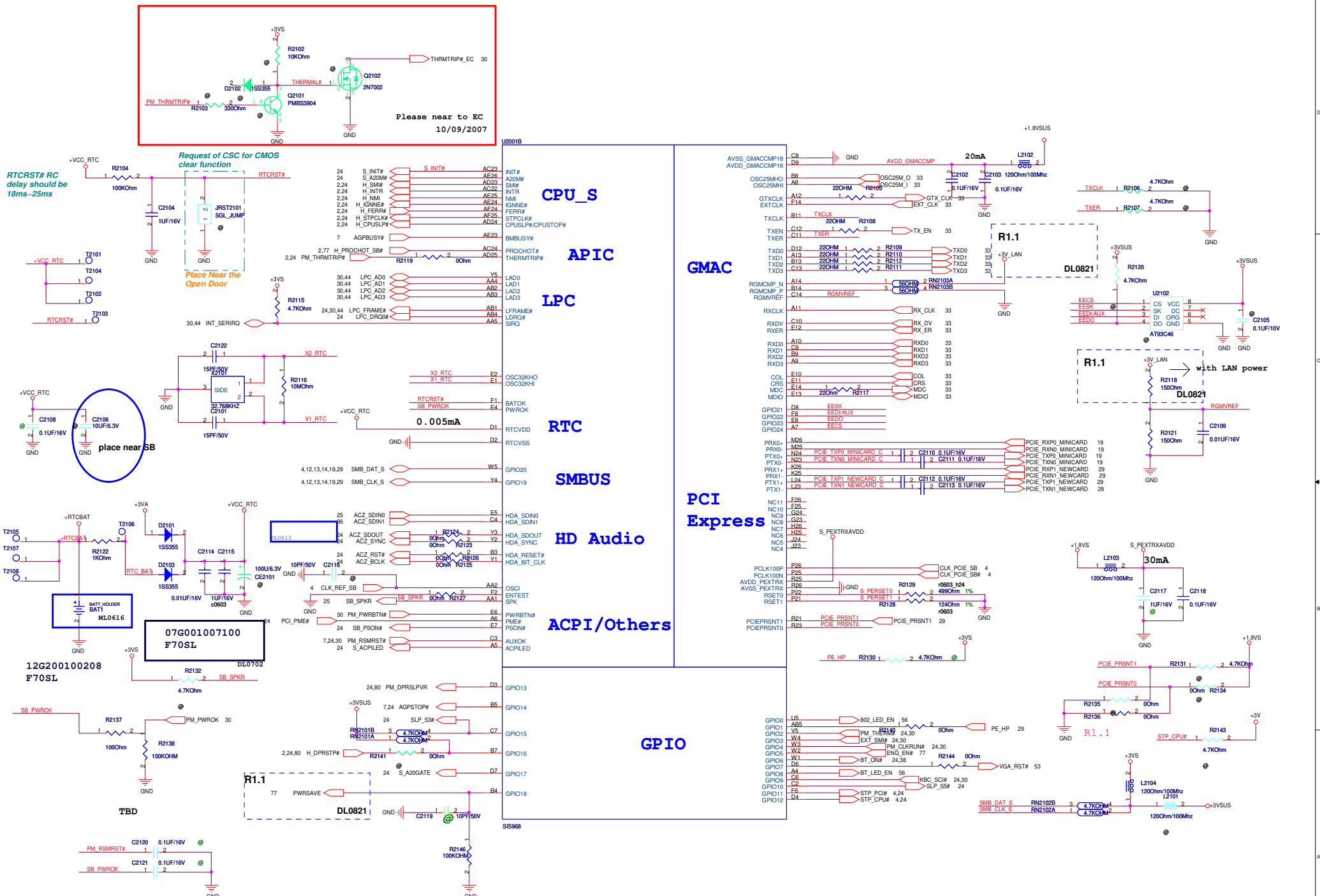


N\_ZA0[16:0] 7



0:LPC ROM 1:SPI ROM









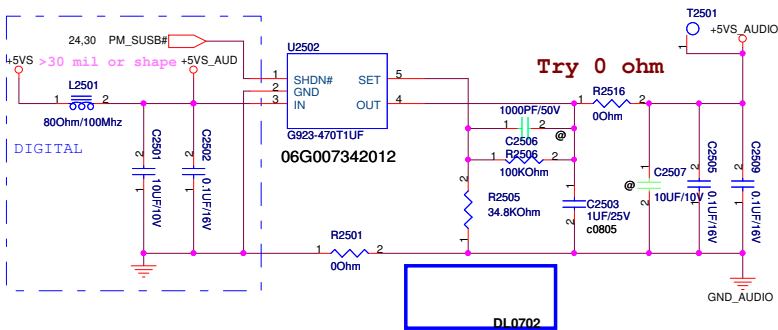




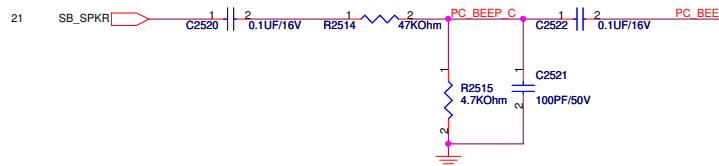
## Audio Power

FOR ADJUST MODE:

$$V_o = 1.25 * (1 + R2506/R2505) \\ = 1.25 * (1 + 100K/34.8K) = 4.84$$



## PC BEEP



# Main Board

Internal Speaker Conn.

12G171010024  
F70SL

FOR EMI

DL0708

12G140301085  
F70SL

DL0617

12G14000106M  
F70SL

DL0630

12G14000106M  
F70SL

DL0630

GAINUG	GAINI	Av (Inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

Reserved for 3G

Reserved for EMI

Delete HP2\_JD circuit

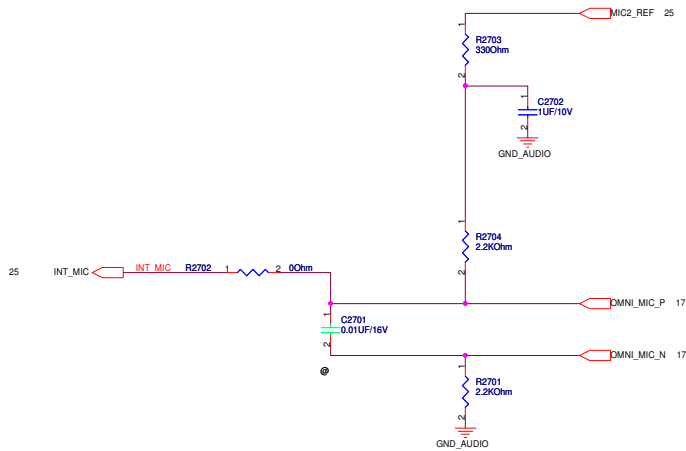
DL0625

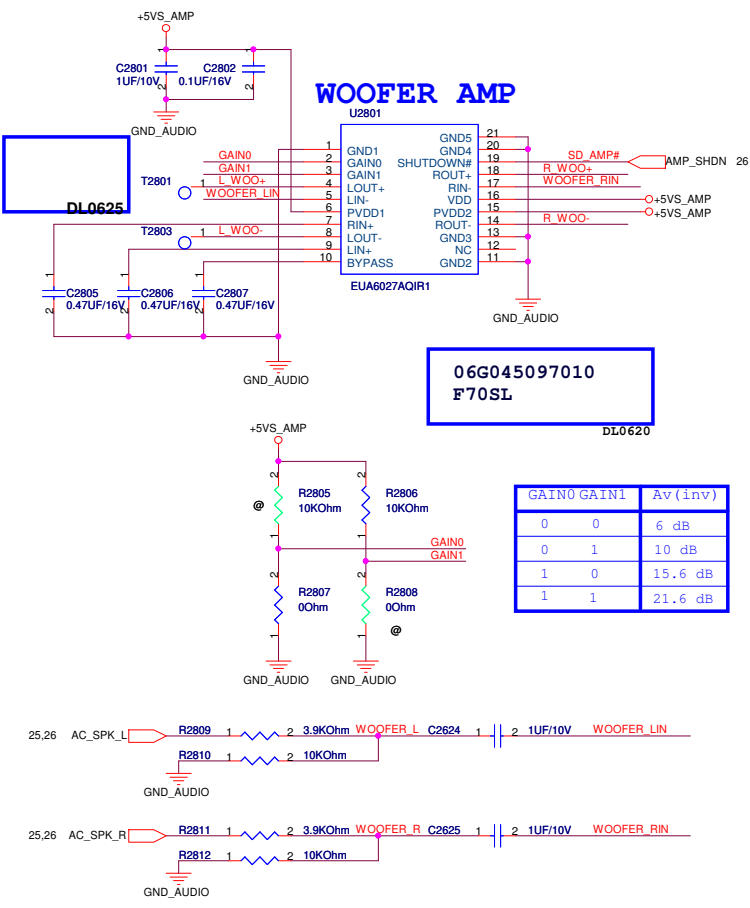
07G003039010  
F70SL

DL0707

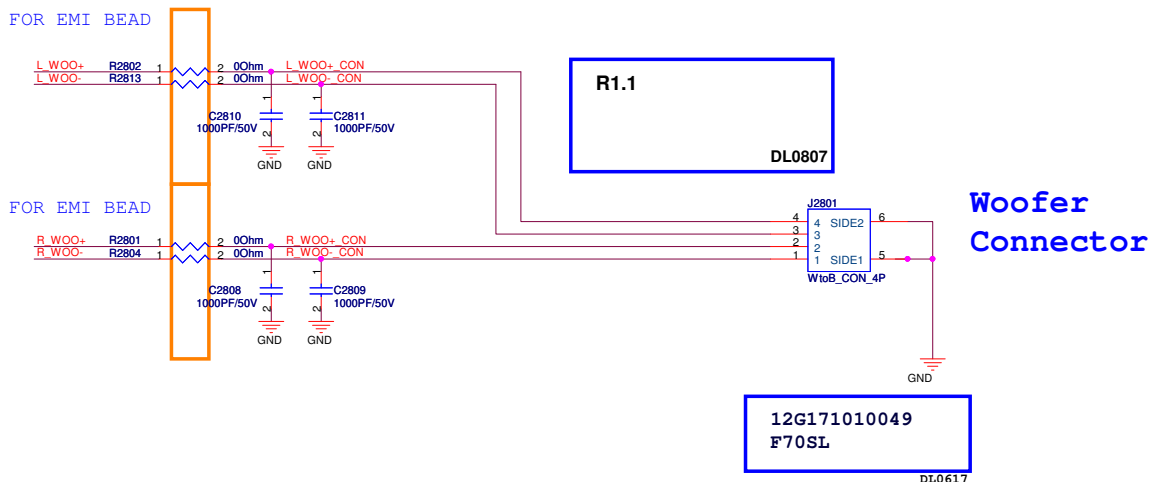
<Variant Name>

ASUS		Title : AUDIO AMP & JACK	
ASUSTek COMPUTER INC. NB1		Engineer: Miller / Daniel	
Size	Project Name	Rev	
C	F70SL	1.0	
Date: Tuesday, November 04, 2008		Sheet 26 of 94	

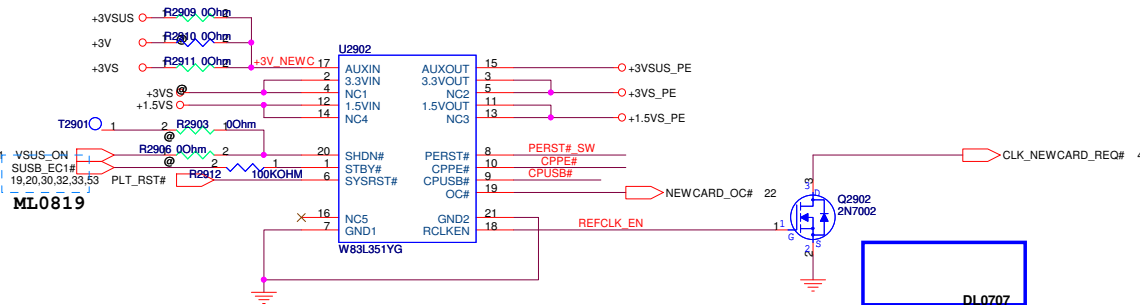
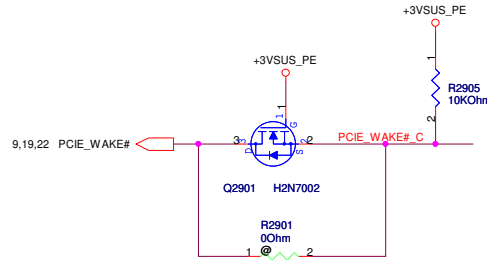
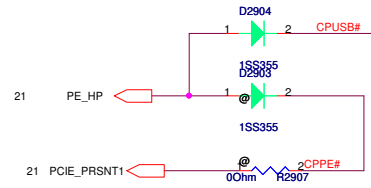
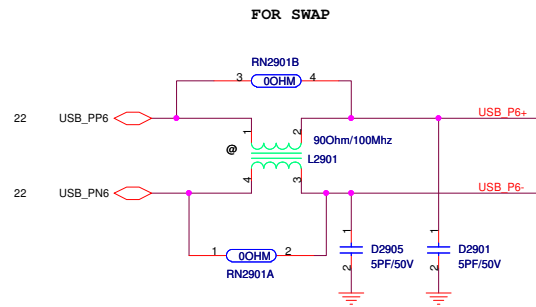




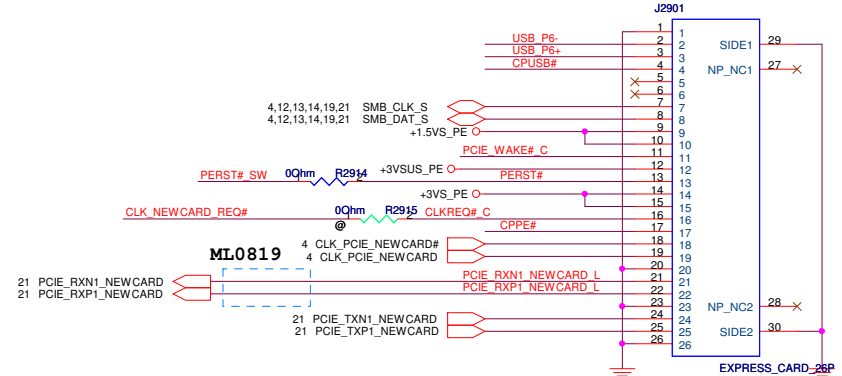
## SPEAKER CONNECTOR WOOFER



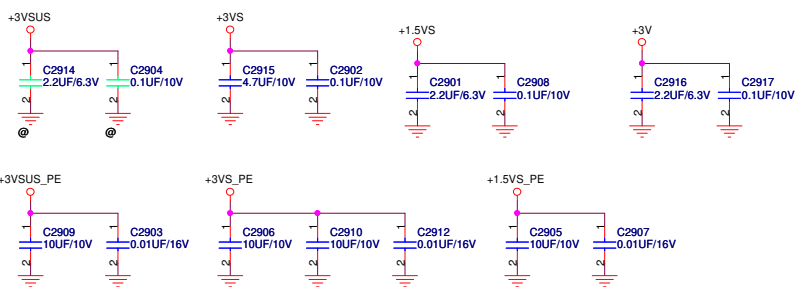
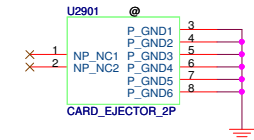
ASUS		Title :Woofer	
ASUSTek COMPUTER INC. NB1		Engineer: Miller / Daniel	
Size	Project Name	Rev	
Custom	F70SL	1.0	
Date: Monday, November 03, 2008		Sheet	28 of 94



**!ExpressCard Standard 1.0:**  
 Change Pin7 from RESERVED to SMBCLK  
 Change Pin8 from SMBCLK to SMBDATA  
 Change Pin9 from SMBDATA to +1.5V



12G161320266  
 F70SL





## For Battery

### Single Battery

BAT1\_CNT1#, BAT1\_CNT2#,  
BAT2\_CNT1#, BAT2\_CNT2#  
don't connect to Battery  
Connector.

### Dual Battery

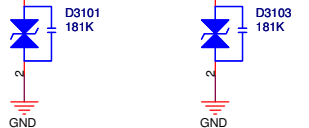
BAT1\_CNT1#, BAT1\_CNT2#,  
BAT2\_CNT1#, BAT2\_CNT2#  
must connect to Battery  
Connector.

#### Note:

When we plug in or plug out the  
battery, it may cause a spike to  
damage the EC and gas gauge. It  
needed to add these varistors to  
protect those pins.

close to connector

R2.0



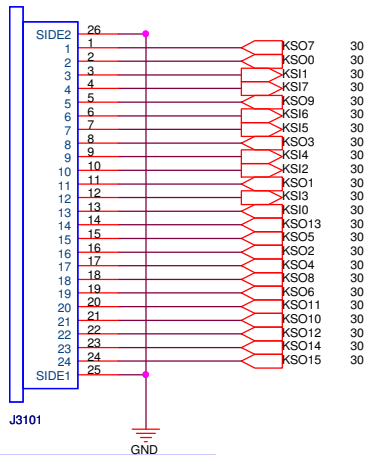
PLACE NEAR J6802

DL0926

## For External PS/2 I/F

### For Keyboard

FPC\_CON\_24P

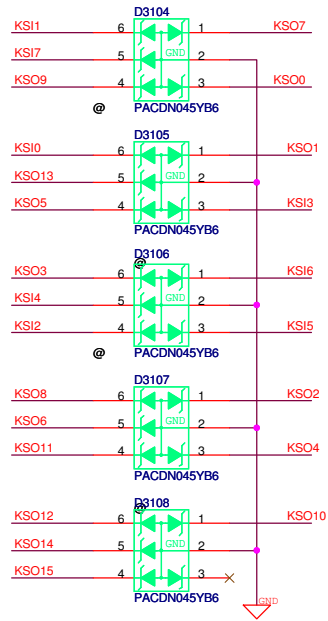


J3101

R1.1  
12G182102402  
F70SL

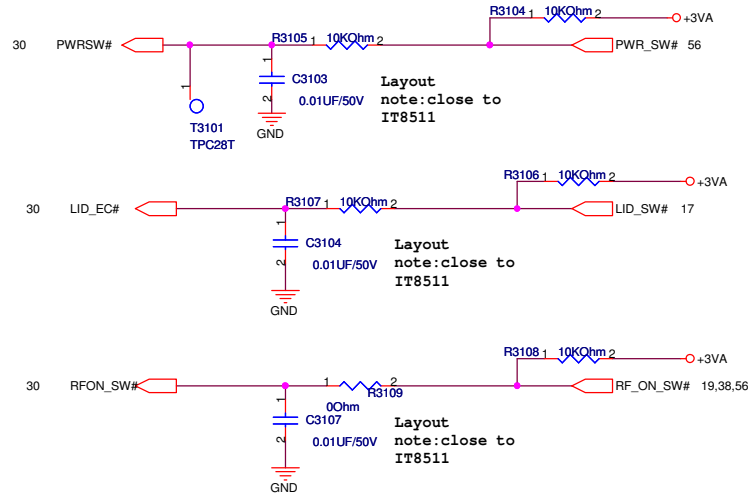
DL0810

EMI recommendation. To protect KBC destroy by ESD.  
Need put between KB connector and KBC, and close to  
the connector as possible.



Each IC needs 2 vias to ground.

## For Switch



PWR  
SWITCH

LID  
SWITCH

RF  
SWITCH

#### Note:

This LID\_EC# is a signal  
from inverter board, it is  
easy to cause high voltage  
damage when plugging  
inverter board connector to  
M/B with AC present. It  
needed to add bidirectional  
diode to protect this pin.

DL0625

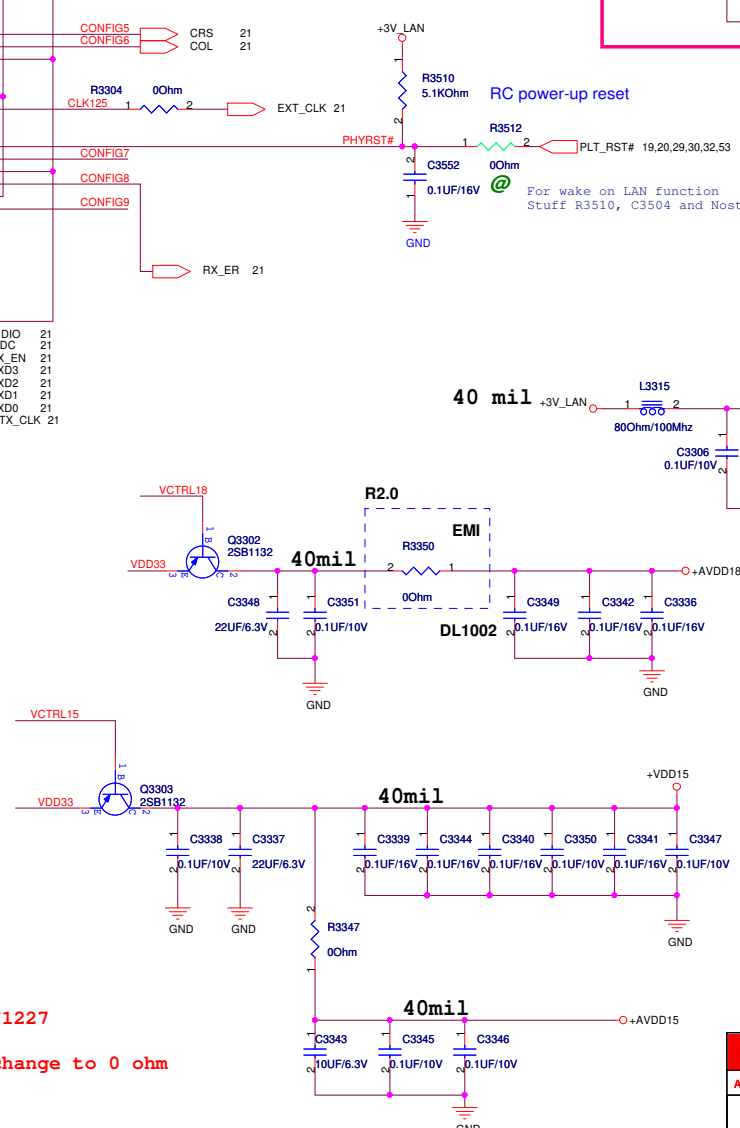
<Variant Name>


<b>ASUS</b>		Title : KB&ISA ROM	
ASUSTeK COMPUTER INC. NB1		Engineer: Miller / Daniel	
Size Custom	Project Name F70SL	Rev 1.0	
Date: Monday, November 03, 2008		Sheet	31 of 94





The schematic diagram illustrates the electrical connections for the DL0702 module. The module is shown as a blue rectangular component with four pins. Pin 1 is connected to the XIN\_LAN signal line and is also connected to a 25Mhz crystal (X3301) and a 27PF/50V capacitor (C3302). Pin 2 is connected to the XOUT\_LAN signal line and is also connected to a 27PF/50V capacitor (C3301). Pin 3 is connected to the GND (ground) plane. Pin 4 is connected to the OSC25M\_O 21 signal line and is also connected to a 25Mhz crystal (X3302) and a 27PF/50V capacitor (C3303). A note 'Place near to 968' is located near the oscillator circuit. The diagram is set against a pink background.

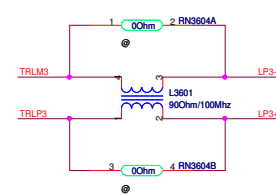
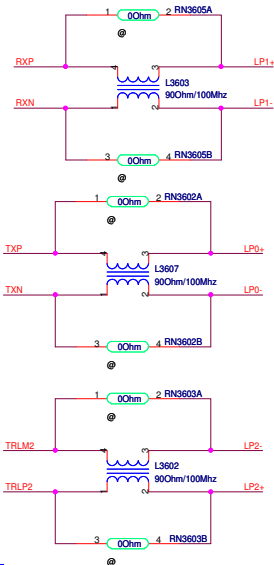
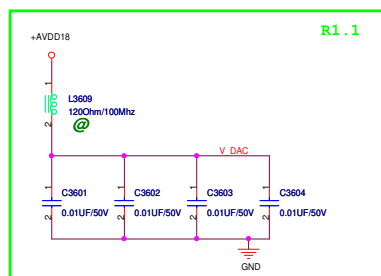
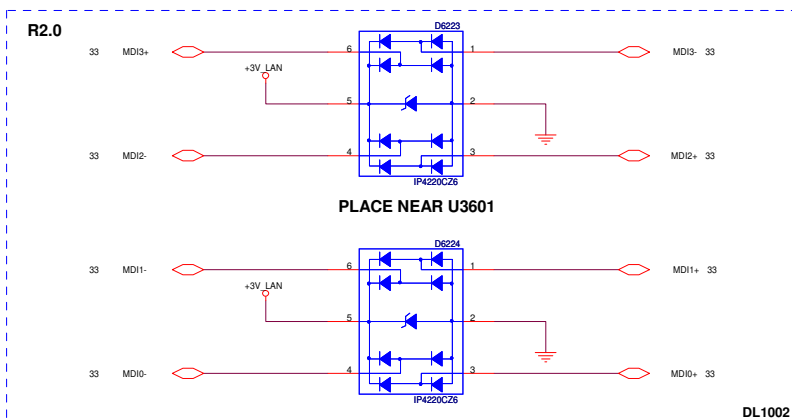
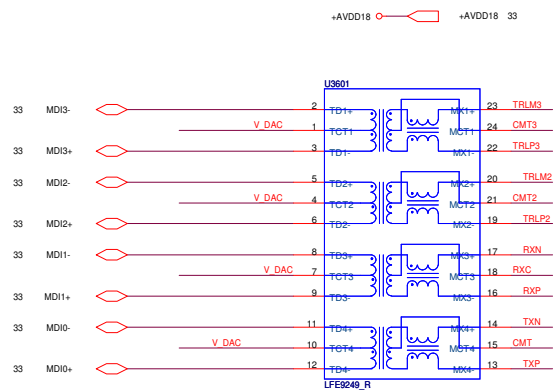


		<b>Title :</b> Giga LAN RTL8211
ASUSTECH CO.,LTD.		<b>Engineer:</b> <i>Miller / Daniel</i>
Size Custom	Project Name  <b>F70SL</b>	Rev 1.1
Date:   Monday, November 03, 2008		Sheet     33     of     94

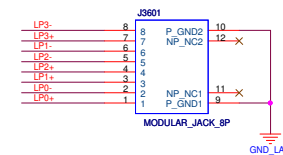


	5	4	3	2	1
D					
C					
B					
A					

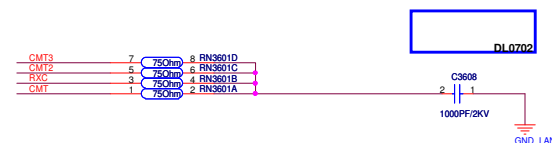
		Title : <b>BLANK</b>	
ASUSTeK Computer INC		Engineer: <b>Miller / Daniel</b>	
Size <b>B</b>	Project Name <b>F70SL</b>		Rev <b>1.0</b>
Date: <b>Monday, November 03, 2008</b>		Sheet <b>35</b> of <b>94</b>	1



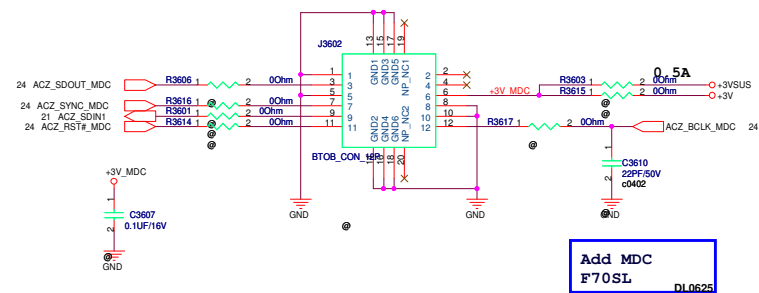
## LAN PORT



**12G14851108M**  
**F70SL**  
**DL0623**

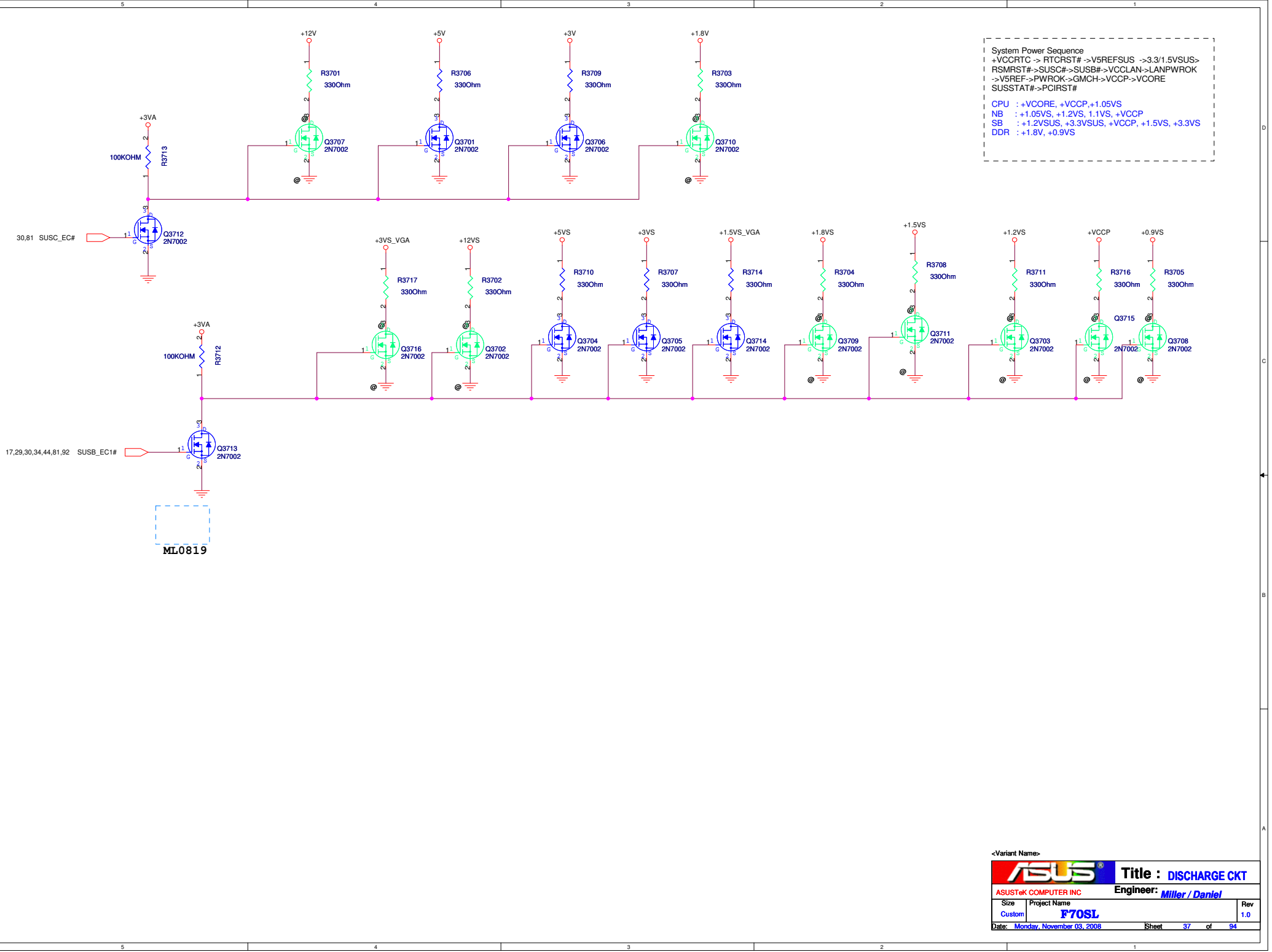


## MDC

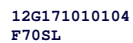


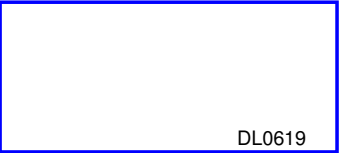
**Add MDC**  
**F70SL**  
**DL0625**





System Power Sequence  
+VCCRTC->RTCST#->V5REFSUS->3.3/1.5VSUS->  
RSMRST#->SUSC#->SUSB#->VCCLAN->LANPWROK  
->V5REF->PWROK->GMCH->VCCP->VCORE  
SUSSTAT#->PCIRST#  
CPU : +VCORE, +VCCP, +1.05VS  
NB : +1.05VS, +1.2VS, 1.1VS, +VCCP  
SB : +1.2VSUS, +3.3VSUS, +VCCP, +1.5VS, +3.3VS  
DDR : +1.8V, +0.9VS





DL0619

<Variant Name>

		Title : SWITCH	
ASUSTeK COMPUTER INC		Engineer: Miller / Daniel	
Size	Project Name		Rev
Custom	F70SL		1.0
Date: Monday, November 03, 2008		Sheet	39 of 94

Delete R5C833

DL0626

<Variant Name>

		Title : R5C833(1)	
ASUSTeK COMPUTER INC. NB1		Engineer: Miller / Daniel	
Size	Project Name		Rev
Custom	F70SL		1.0
Date: Monday, November 03, 2008		Sheet	40 of 94



Delete R5C833

DL0626

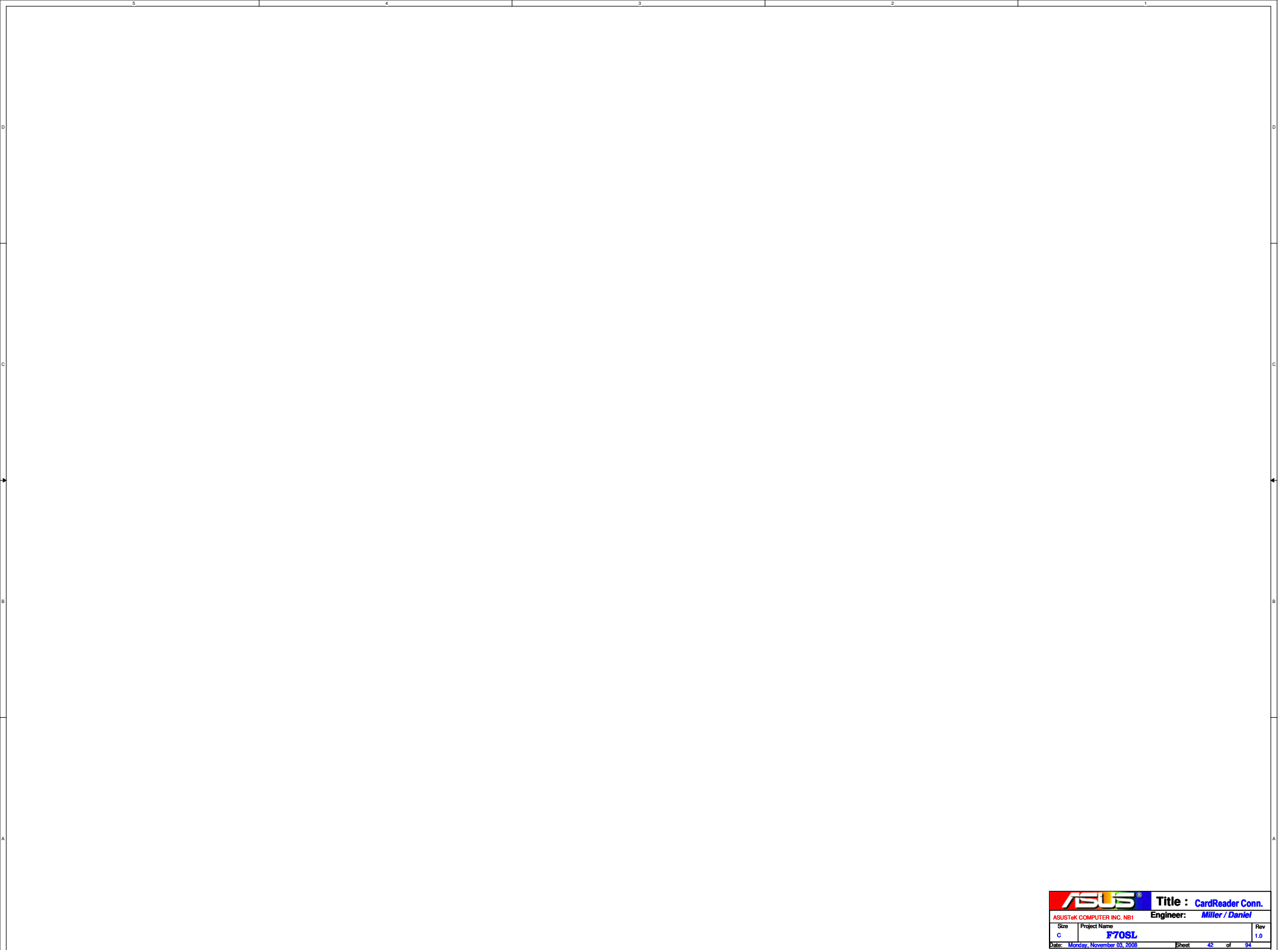


**Title :** R5C833(2)

ASUSTeK COMPUTER INC. NB1

Engineer: *Miller / Daniel*

Size Custom	Project Name <b>F70SL</b>	Rev 1.0
Date: Monday, November 03, 2008		Sheet 41 of 94



		<b>Title :</b> CardReader Conn.	
ASUSTAK COMPUTER INC. NBY		<b>Engineer:</b> Miller / Daniel	
Size	Project Name		Rev
C	F70SL		1.0
Date: Monday, November 03, 2008		Sheet	42 of 64







		<b>Title :</b> N/A	
ASUSTeK COMPUTER INC		<b>Engineer:</b> Miller / Daniel	
Size	Project Name		Rev
C	<b>F70SL</b>		1.0
Date: Monday, November 03, 2008		Sheet 45 of	94

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

		<b>Title :</b> N/A	
<small>ASUSTeK COMPUTER INC</small>		<b>Engineer:</b> Miller / Daniel	
Size C	Project Name <b>F70SL</b>	Rev 1.0	
<small>Date: Monday, November 03, 2008</small>		Sheet 46 of 94	

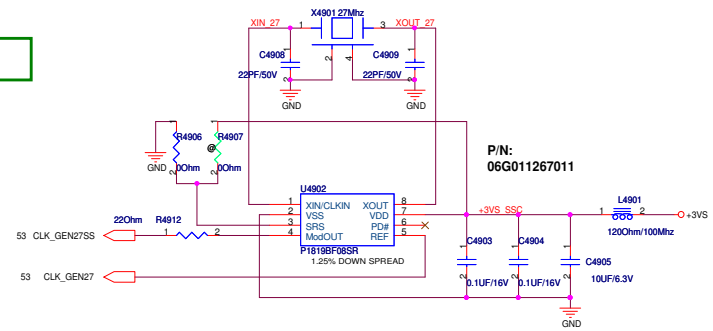


		<b>Title :</b> N/A	
ASUSTeK COMPUTER INC		<b>Engineer:</b> Miller / Daniel	
Size C	Project Name <b>F70SL</b>		Rev 1.0
Date: Monday, November 03, 2008		Sheet 47	of 94





XTAL\_IN , XTAL\_OUT  
3.3V tolerance



	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

		<b>Title :</b> N/A	
<small>ASUSTeK COMPUTER INC</small>		<b>Engineer:</b> Miller / Daniel	
Size C	Project Name <b>F70SL</b>	Rev 1.0	
<small>Date: Monday, November 03, 2008</small>		Sheet 50 of 94	

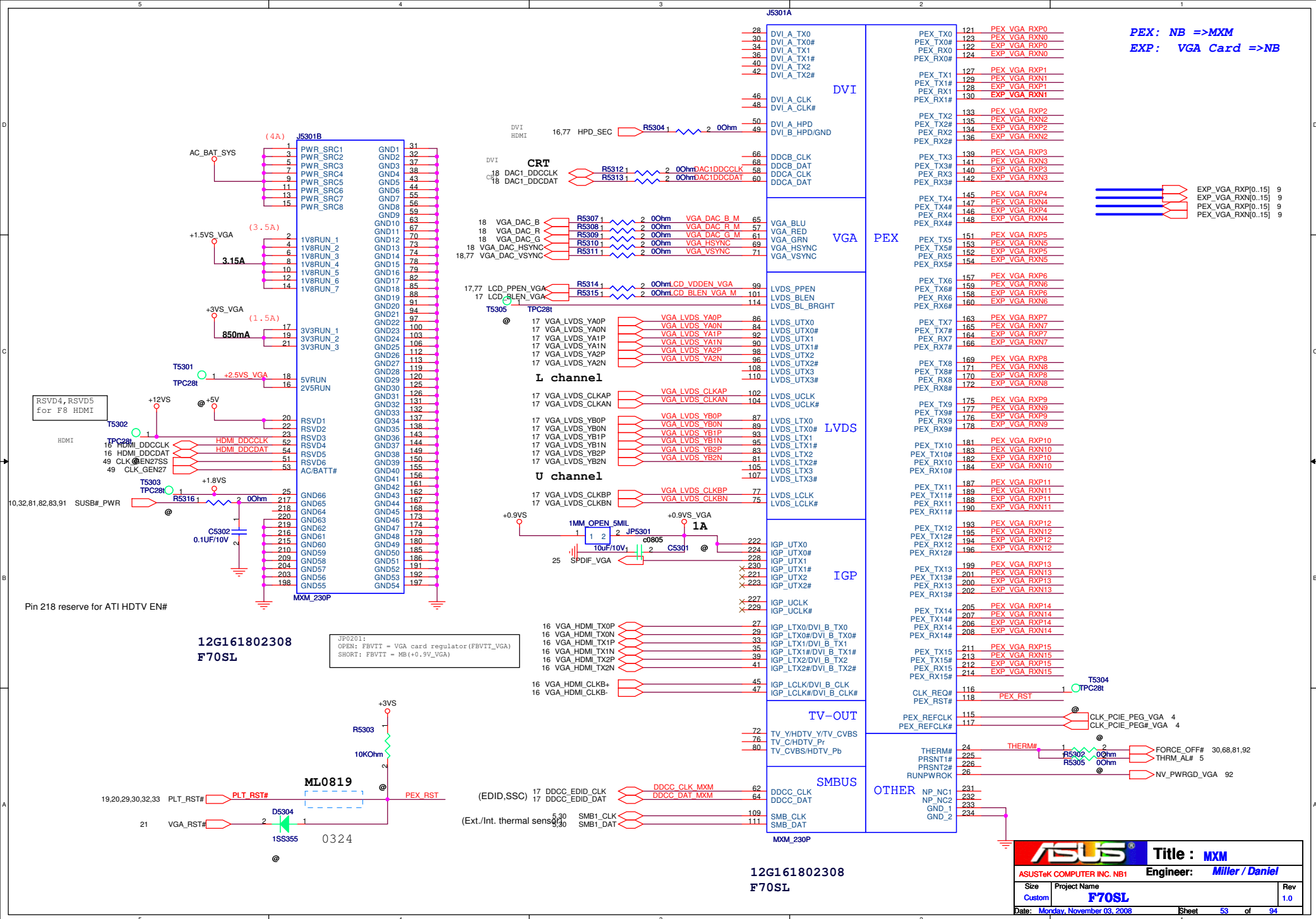


		<b>Title :</b> N/A	
ASUSTeK COMPUTER INC		<b>Engineer:</b> Miller / Daniel	
Size	Project Name		Rev
C	<b>F70SL</b>		1.0
Date: Monday, November 03, 2008		Sheet	51 of 94



DL0011

		Title : N/A	
ASUSTAK COMPUTER INC		Engineer: Miller / Daniel	
Size	Project Name		Rev
C	F70SL		1.0
Date: Monday, November 03, 2008		Sheet	52 of 84



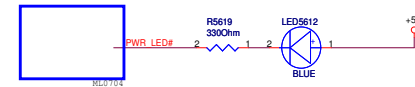
	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

		Title : <b>BLANK</b>	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Miller / Daniel</i>	
Size <b>A</b>	Project Name <b>F70SL</b>		Rev <b>1.0</b>
Date: <b>Monday, November 03, 2008</b>		Sheet	<b>54</b> of <b>94</b>

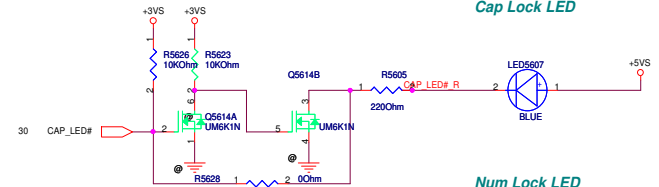


		<b>Title :</b> SS STRAPS	
ASUSTeK COMPUTER INC. NB1		<b>Engineer:</b> Miller / Daniel	
Size	Project Name		Rev
Custom	F70SL		1.0
Date: Monday, November 03, 2008		Sheet	55 of 94

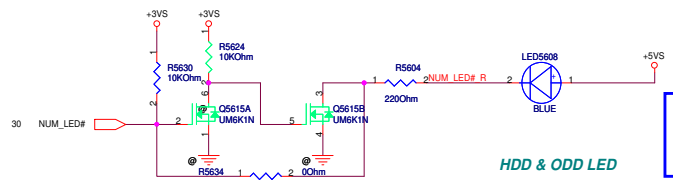
## Power LED



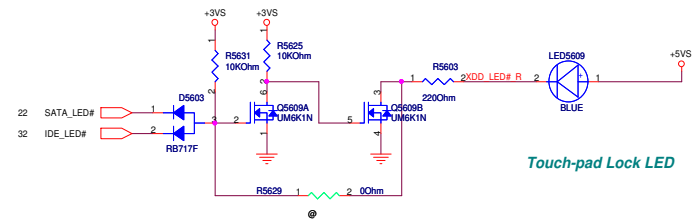
## Cap Lock LED



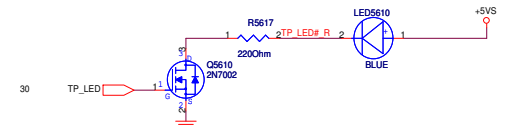
## Num Lock LED



## HDD &amp; ODD LED



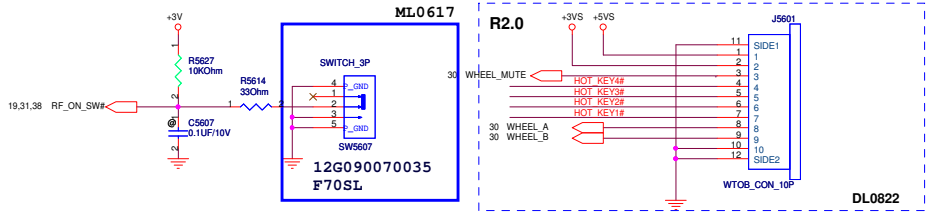
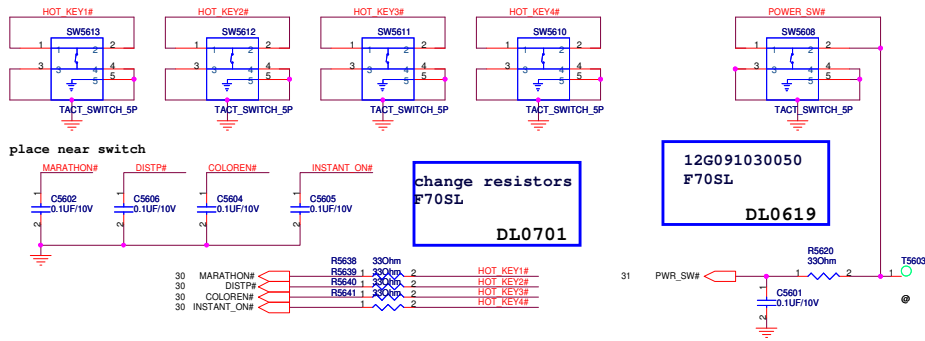
## Touch-pad Lock LED



R1.1

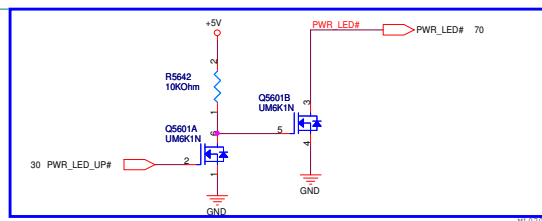
DELETE MAIL LED CIRCUIT

DL0810

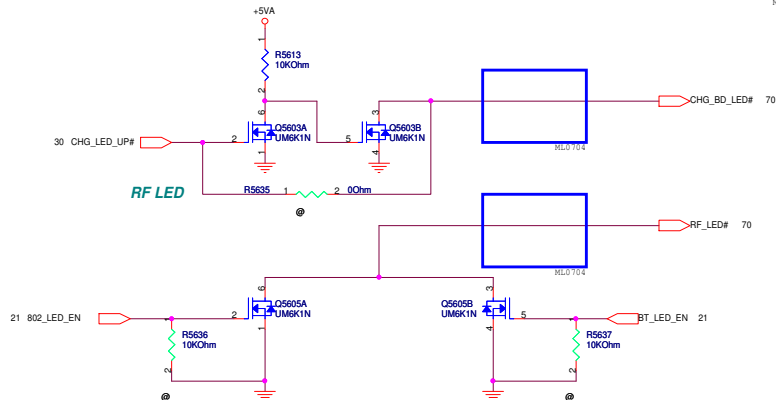


## Power LED

## Charger LED



## RF LED







**Title : +1.2VSUS**

ASUSTeK COMPUTER INC. NB1

**Engineer:** *Miller / Daniel*

Size  
A

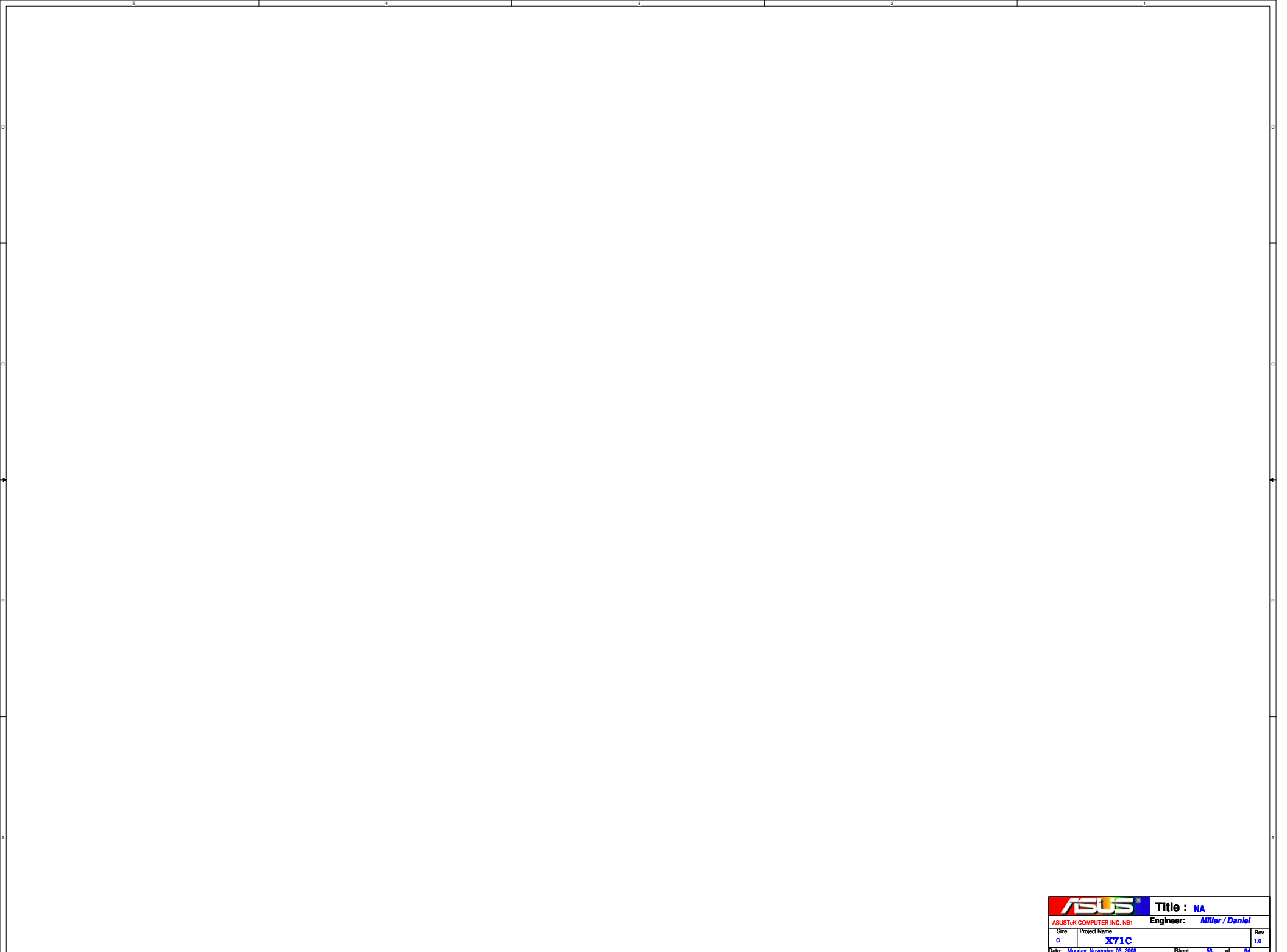
Project Name
--------------

**F70SL**

Rev
1.0

Date: Monday, November 03, 2008

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		Title : <b>NA</b>	
ASUSTeK COMPUTER INC. NB1		Engineer: <b>Miller / Daniel</b>	
Size	Project Name		Rev
C	<b>X71C</b>		1.0
Date: <b>Monday, November 03, 2008</b>		Sheet <b>58</b> of <b>94</b>	



**Title :** EMI

ASUSTeK COMPUTER INC. NB1

**Engineer:** *Miller / Daniel*

Size  
A

Project Name
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**F70SL**

Rev
1.0

Date: Monday, November 03, 2008

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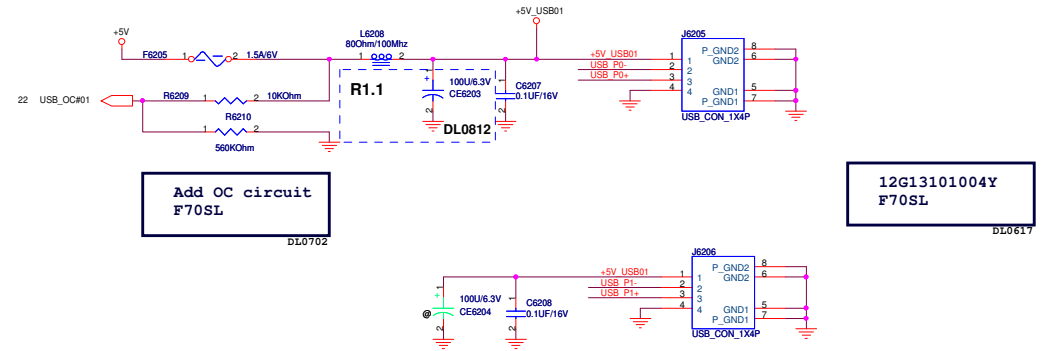
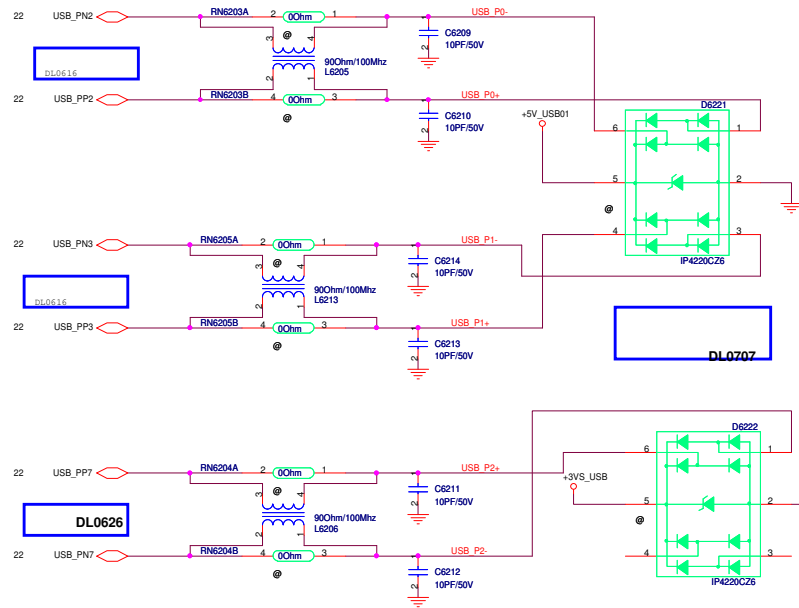
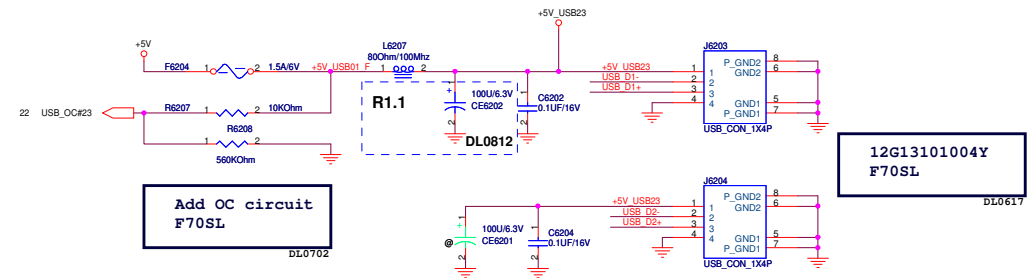
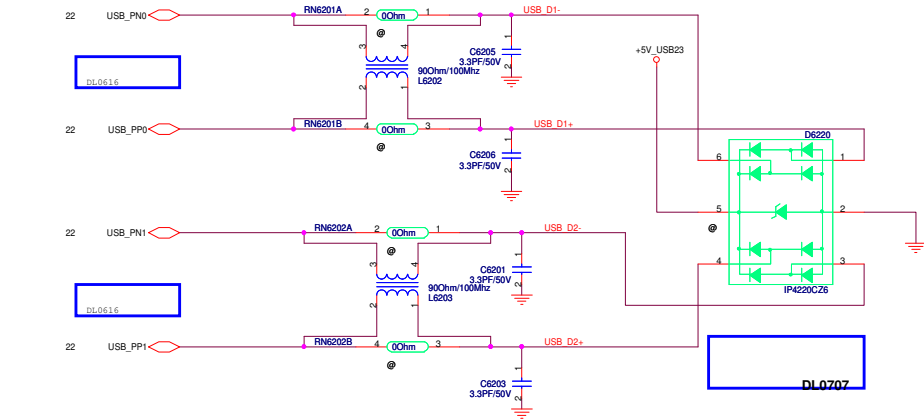
Delete SPIF215A

DL0626

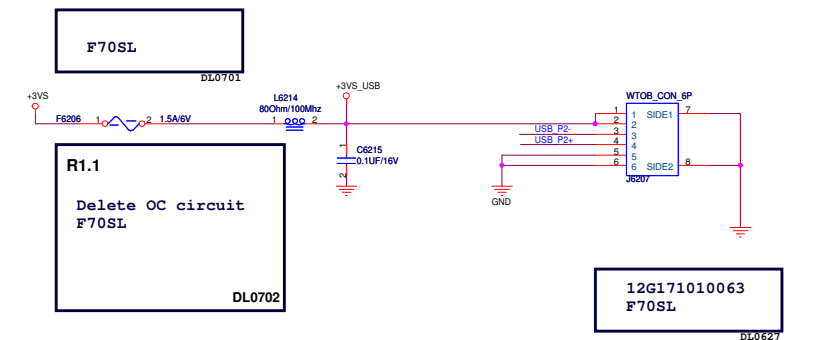
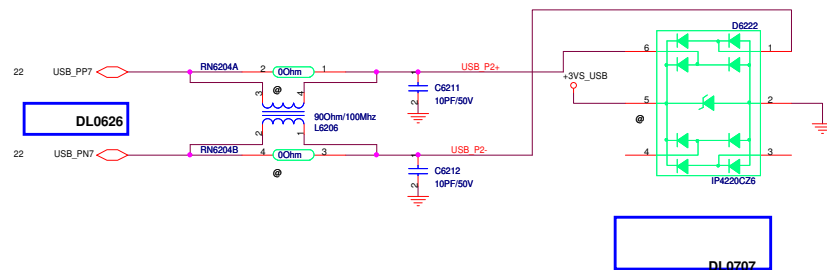
		Title : USB SATA adapter	
ASUSTeK COMPUTER INC. NB1		Engineer: Miller / Daniel	
Size	Project Name		Rev
C	F70SL		1.0
Date: Monday, November 03, 2008		Sheet	60 of 94

DL0616

		<b>Title :</b> USB HUB	
ASUSTeK COMPUTER INC. NB1		<b>Engineer:</b> Miller / Daniel	
Size B	Project Name <b>F70SL</b>		Rev 1.0
Date: Monday, November 03, 2008		Sheet 61 of 94	



## CardReader Connector




<Variant Name>

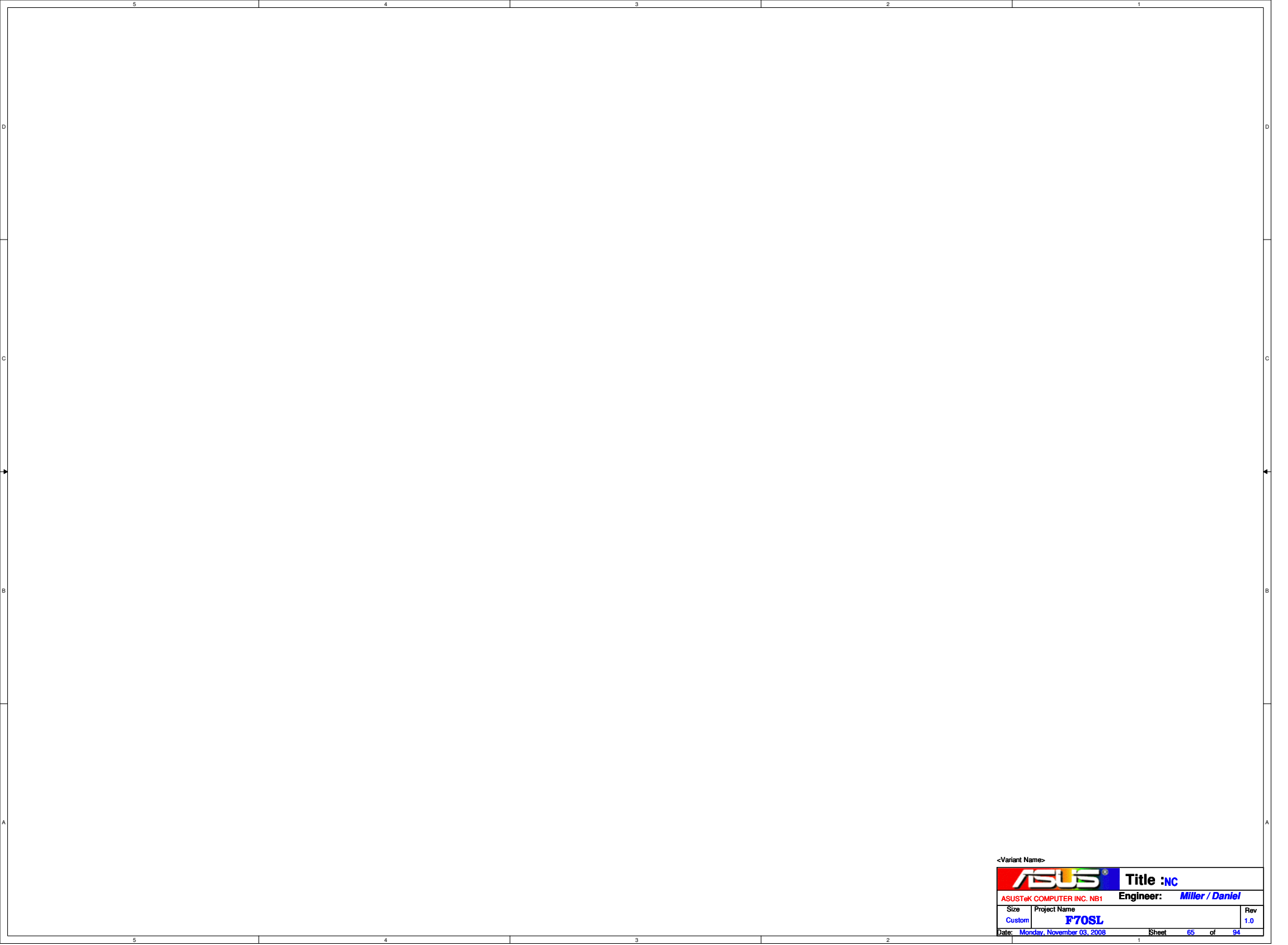
ASUS		Title : USB CONN	
ASUSTeK COMPUTER INC		Engineer: Miller / Daniel	
Size	Project Name	Rev	
C	F70SL	1.0	
Date: Thursday, November 13, 2008		Sheet 62 of 94	



	5	4	3	2	1	
D						D
C						C
B						B
A						A
	5	4	3	2	1	

		Title : <b>BLANK</b>	
ASUSTeK COMPUTER INC. NB1		Engineer: <b>Miller / Daniel</b>	
Size <b>A</b>	Project Name <b>F70SL</b>		Rev <b>1.0</b>
Date: <b>Monday, November 03, 2008</b>		Sheet	<b>64</b> of <b>94</b>





<Variant Name>			
		Title : <b>NC</b>	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Miller / Daniel</i>	
Size	Project Name		Rev
Custom	<b>F70SL</b>		1.0
Date: <u>Monday, November 03, 2008</u>		Sheet	65 of 94

		<b>Title :</b> NC	
ASUSTek COMPUTER INC. NB1		<b>Engineer:</b> <i>Miller / Daniel</i>	
Size Custom	Project Name <b>F70SL</b>	Rev <b>1.0</b>	
Date: Monday, November 03, 2008		Sheet 66 of 94	

D

C

B

A



**Title :** BLANK

ASUSTeK COMPUTER INC. NB1

Engineer: **Miller / Daniel**

Size  
A

Project Name
--------------

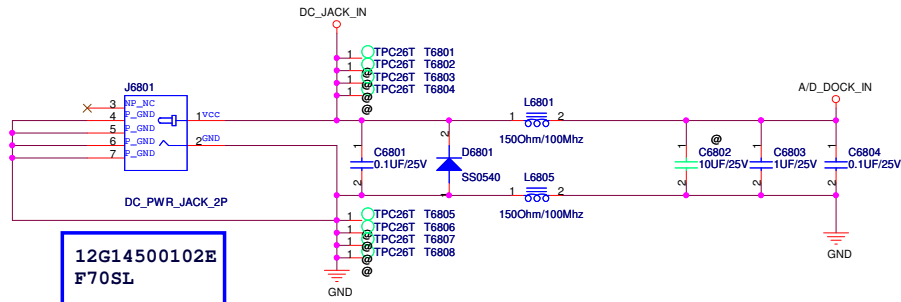
**F70SL**

Rev
1.0

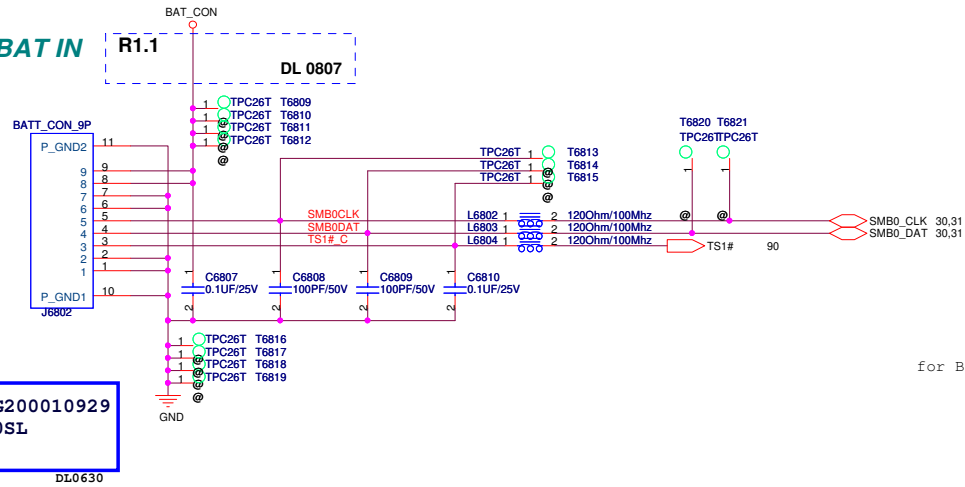
Date: Monday, November 03, 2008

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## DC IN

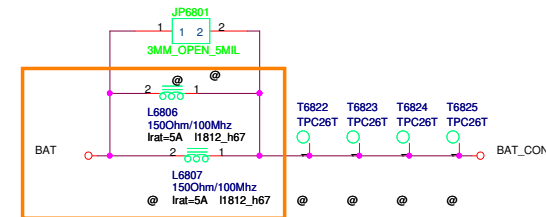


## BAT IN



Add jumper & EMI bead

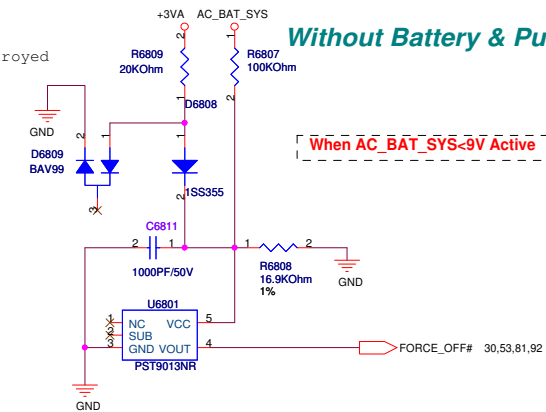
DL0625



for BIOS is destroyed

1/23

Without Battery & Pull out Adapter



<Variant Name>

<b>ASUS</b>		Title : DC & BAT IN	
ASUSTeK COMPUTER INC. NBI		Engineer: Miller / Daniel	
Size	Project Name	Rev	
Custom	F70SL	1.0	
Date: Monday, November 03, 2008	Sheet	68	of 94



**Title : BLANK**

ASUSTeK COMPUTER INC. NB1

**Engineer:** *Miller / Daniel*

Size  
A

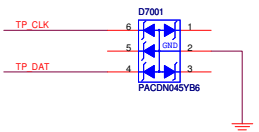
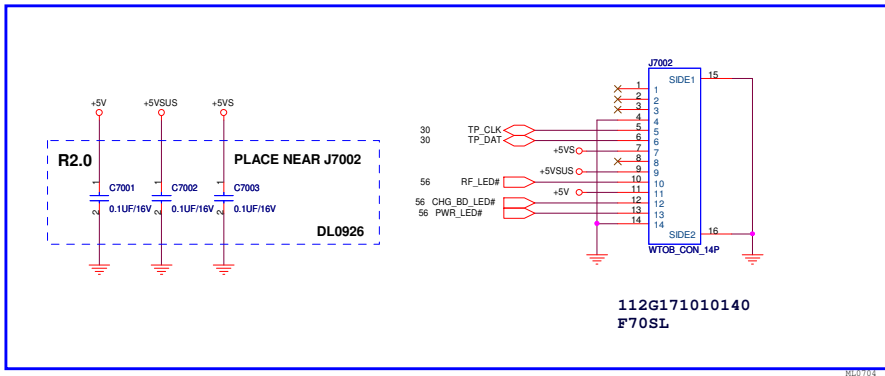
Project Name
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**F70SL**

Rev
1.0

Date: Monday, November 03, 2008

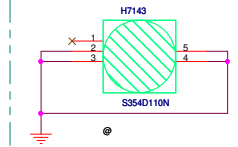
Sheet 69 of 94



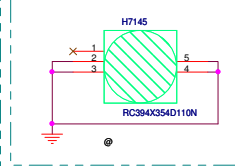
Screw Hole A



Screw Hole B



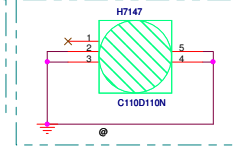
Screw Hole C



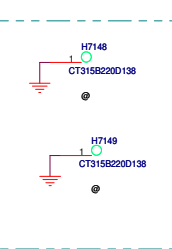
Screw Hole D



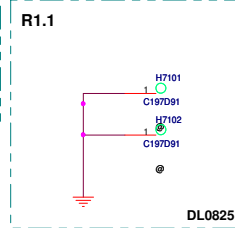
Screw Hole E



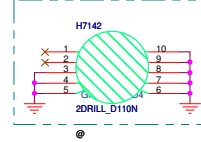
Screw Hole F



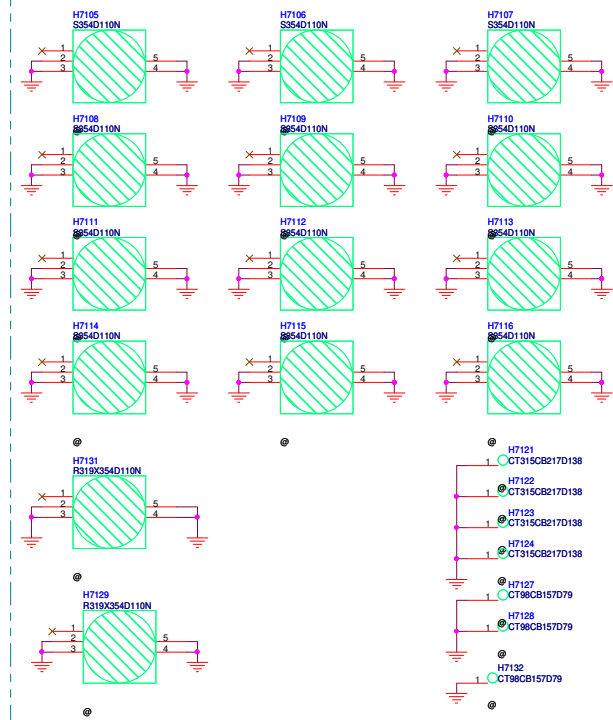
Screw Hole G



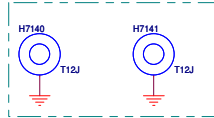
Screw Hole J



F70SL Screw Hole



NUT 2.5H



5						4						3						2						1					
D																								D					
C																								C					
B																								B					
A																								A					





**Title : BLANK**

ASUSTeK COMPUTER INC. NB1

**Engineer:** *Miller / Daniel*

Size  
A

Project Name
--------------

**F70SL**

Rev
1.0

Date: Monday, November 03, 2008

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1.080926 Add C7001,C7002,C7003,D7001 for EMI on Page 70  
2.080926 Add C3238 for EMI on Page 32  
3.080926 place D3101,D3103 near J6802 for EMI on Page 31  
4.080926 Add C8040 near R8001 for EMI on Page 80  
5.080930 Modify Page 32  
6.080930 Add wheel\_mute pin on Page 56  
7.081002 Add R3350,R3351,R3352 for EMI on Page 33

D

C

B

A



**Title : BLANK**

ASUSTeK COMPUTER INC. NB1

**Engineer:** *Miller / Daniel*

Size  
A

Project Name	
--------------	--

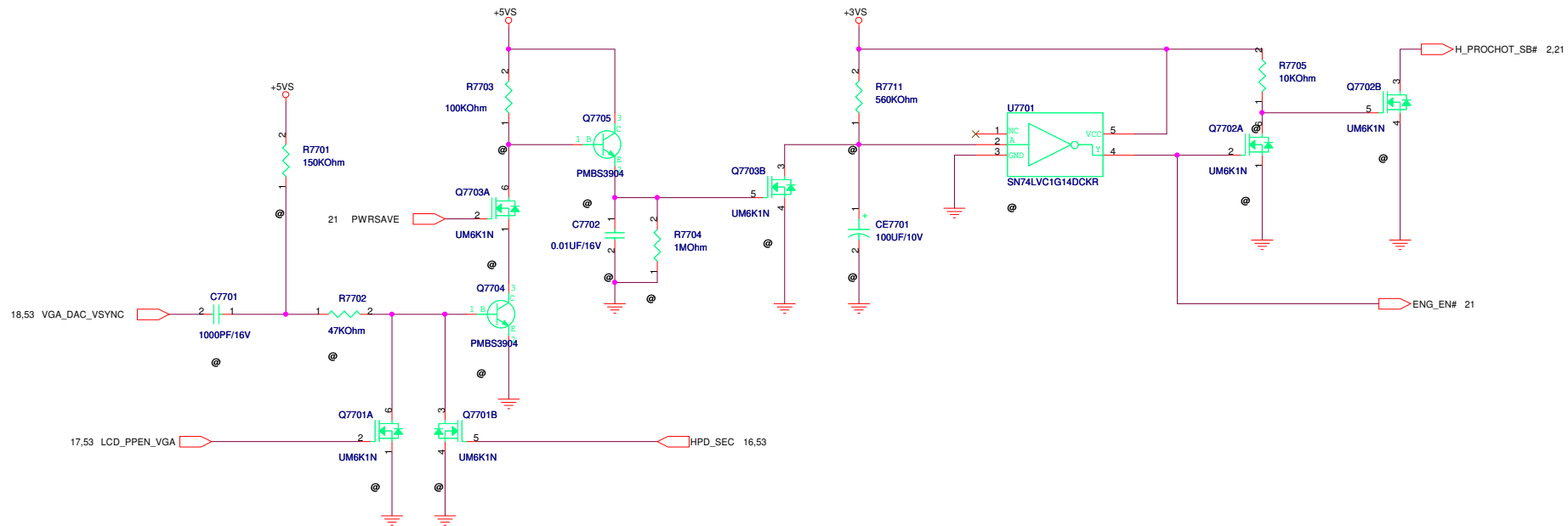
**F70SL**

Rev  
1.0

Date: Monday, November 03, 2008

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		<b>Title :</b> <i>Energy Star</i>	
<b>ASUSTek COMPUTER INC</b>		<b>Engineer:</b> <i>Miller / Daniel</i>	
Size Custom	Project Name  <b>F70SL</b>		Rev 2.1
Date: <i>Monday, November 03, 2008</i>		Sheet 76 of 94	

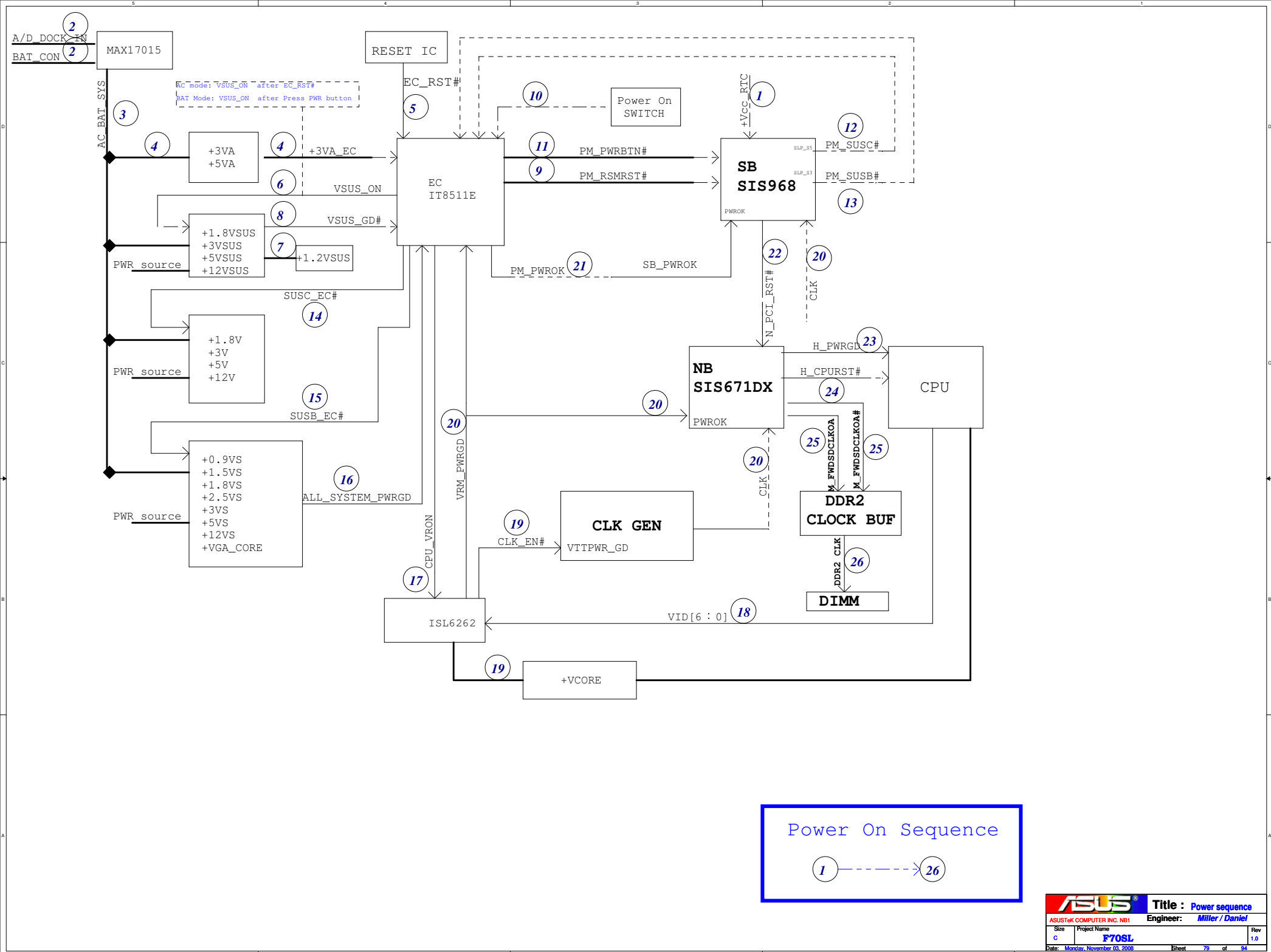


<Variant Name>

<b>ASUS</b>		<b>Title : Battery Saving</b>	
ASUSTeK COMPUTER INC		Engineer: <i>Miller / Daniel</i>	
Size	Project Name		Rev
Custom	<b>F70SL</b>		2.1
Date: Monday, November 03, 2008		Sheet	77 of 94

	5	4	3	2	1	
D						D
C						C
B						B
A						A
	5	4	3	2	1	

		Title : <b>BLANK</b>	
ASUSTeK COMPUTER INC. NB1		Engineer: <b>Miller / Daniel</b>	
Size <b>A</b>	Project Name <b>F70SL</b>		Rev <b>1.0</b>
Date: <b>Monday, November 03, 2008</b>		Sheet <b>78</b> of <b>94</b>	















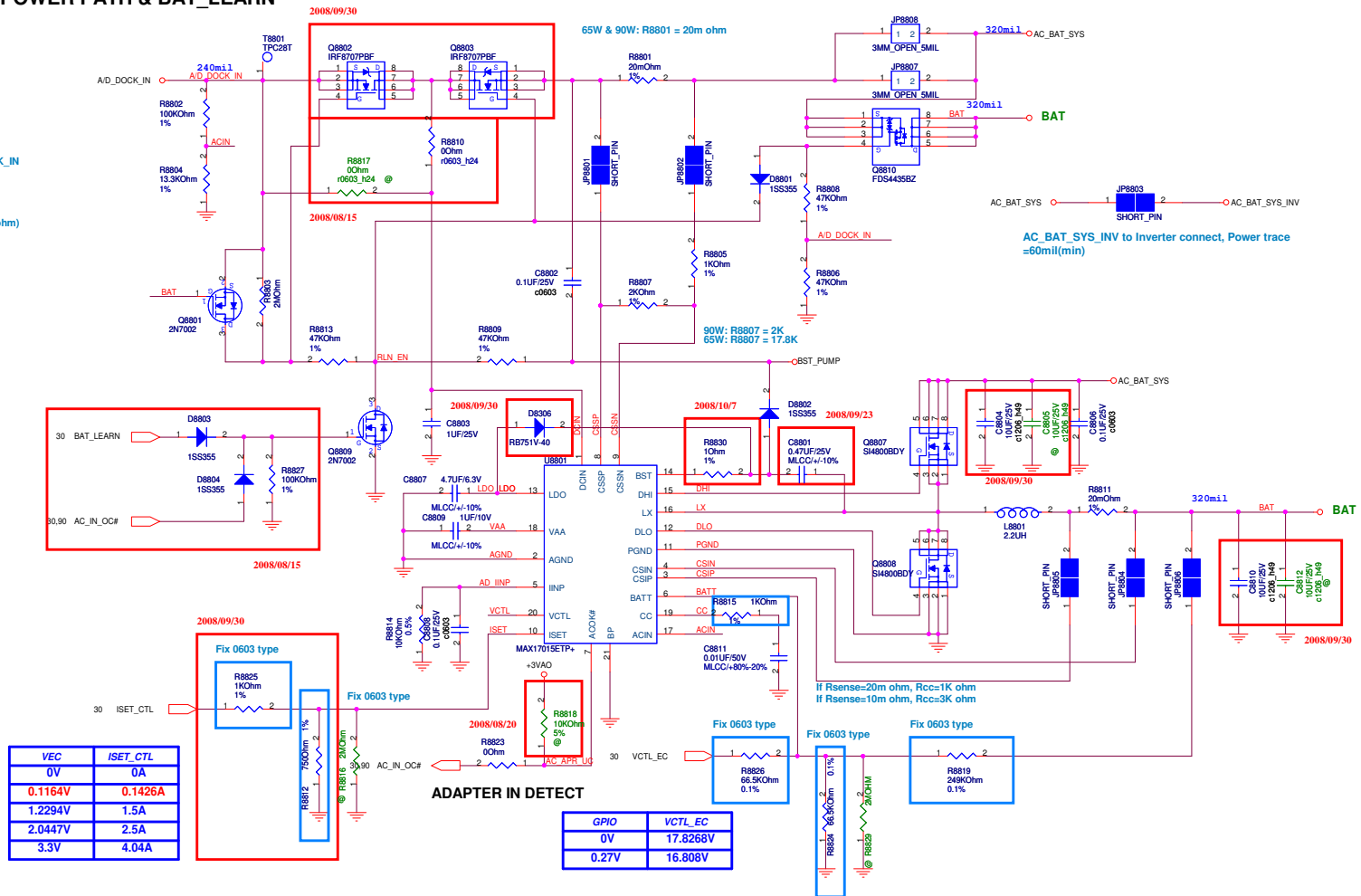


<Variant Name>			
		Title : <b>NA</b>	
<OrgName>		Engineer: <b>Eric_Ho</b>	
Size <b>B</b>	Project Name <b>F70SL</b>		Rev <b>1.0</b>
Date: <b>Monday, November 03, 2008</b>	Sheet	<b>86</b>	of <b>94</b>



AC\_IN Threshold 2.048Vmax A/D\_DOCK\_IN  
> 17.44V active

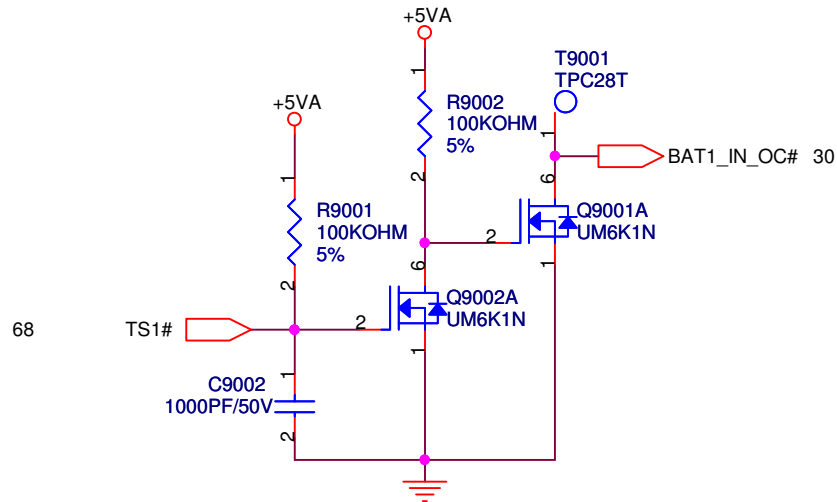
AD\_INP:  
Input =  $V_{iinp}/(R_{S1} \cdot G_{iinp} \cdot R_{iinp})$   
=  $V_{iinp}/(15m\ ohm \cdot 2.8mA/V \cdot 10k\ ohm)$   
= 2.38  $V_{iinp}$



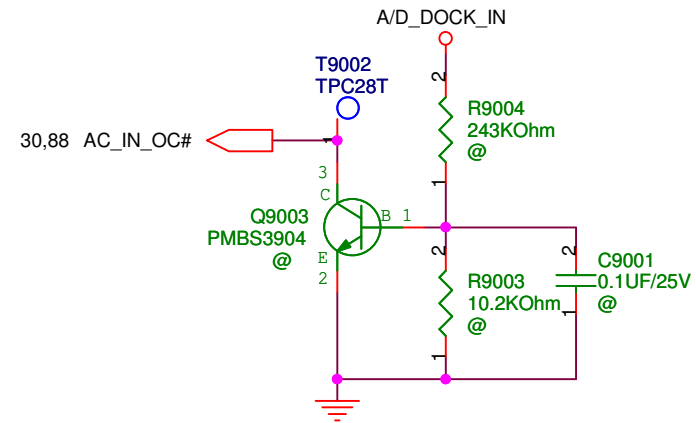




## BATTERY IN DETECT



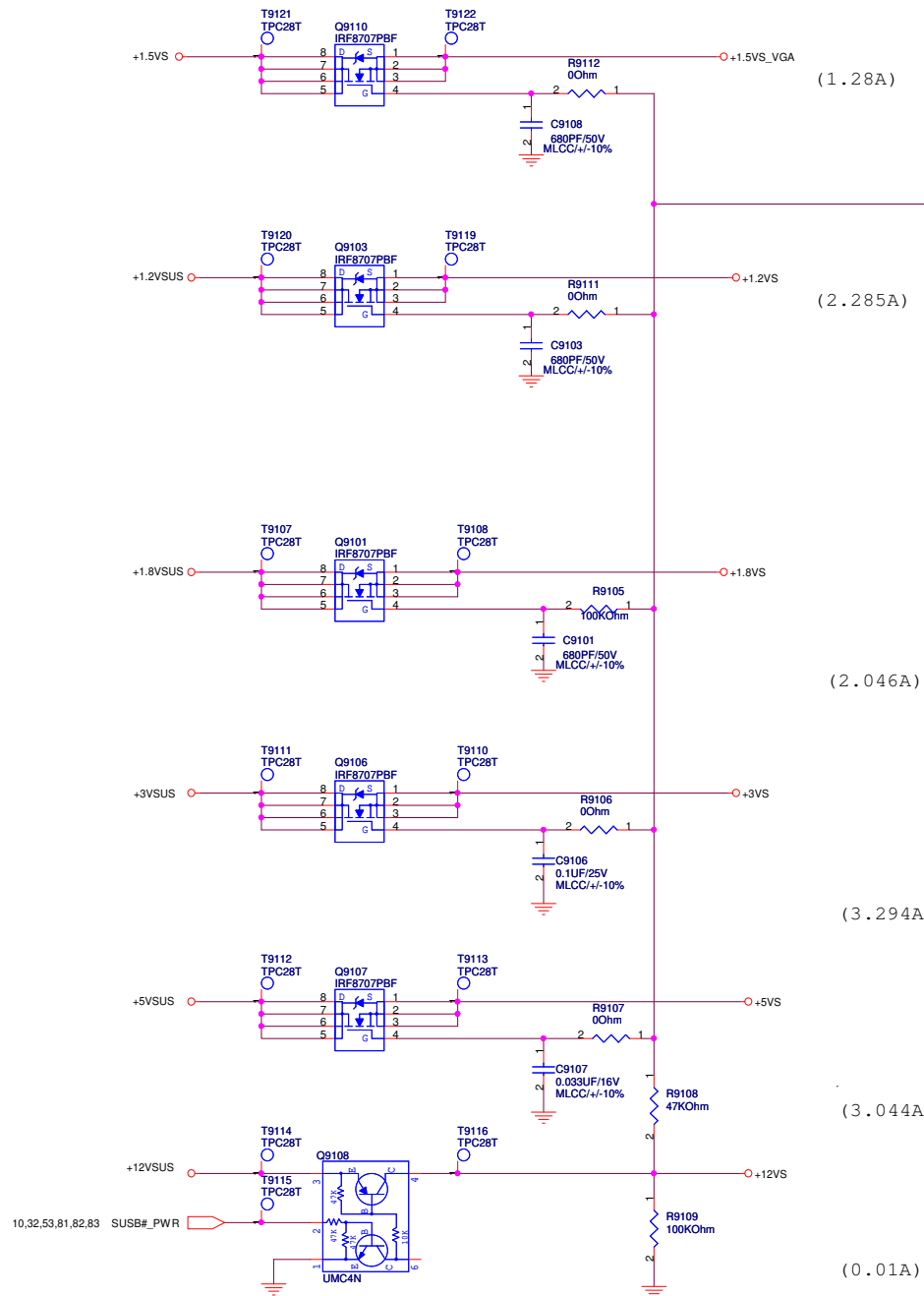
## ADAPTER IN DETECT



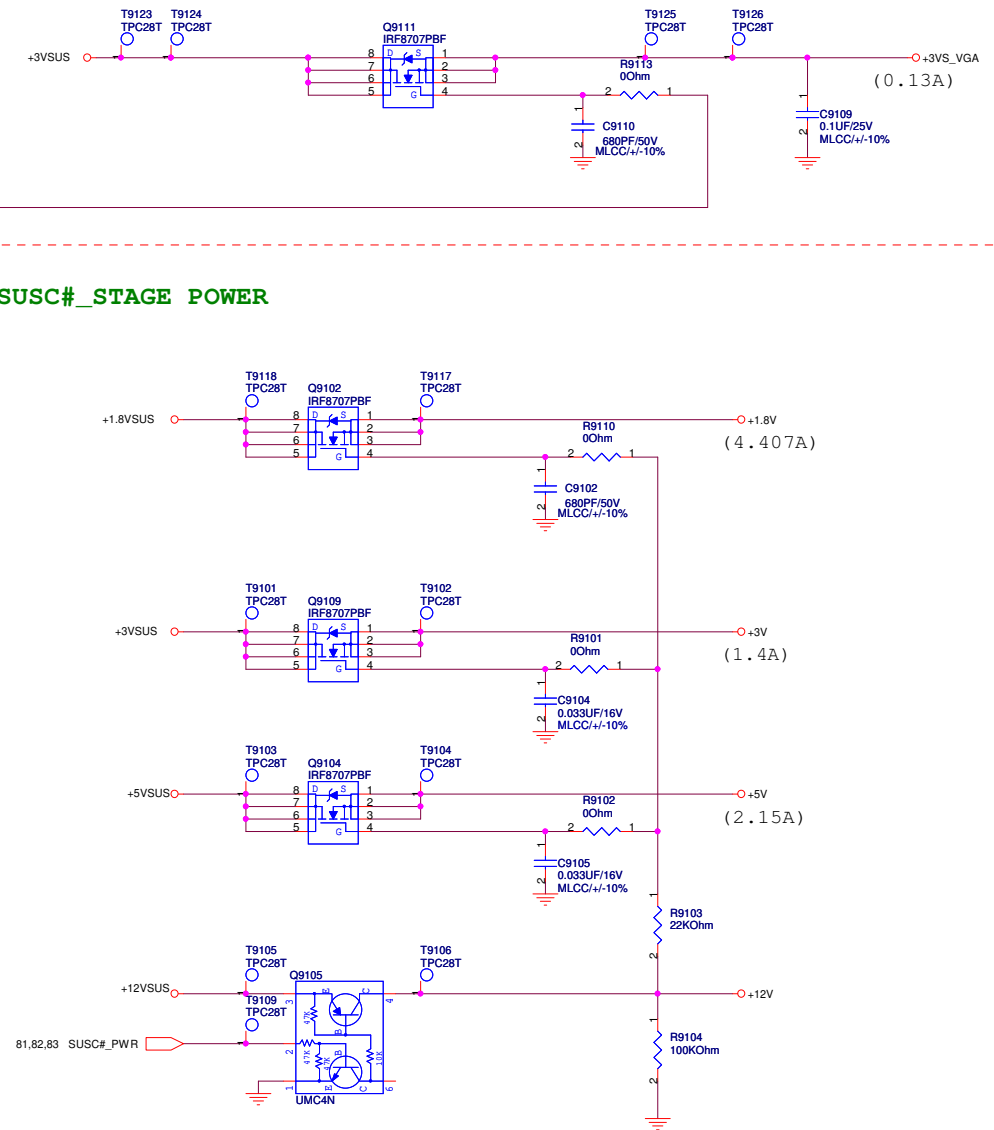
<Variant Name>

<b>ASUS</b>		<b>Title :POWER_DETECT</b>	
<OrgName>		<b>Engineer: Eric_Ho</b>	
Size A	Project Name <b>F70SL</b>		Rev 1.0
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## SUSB#\_STAGE POWER



## SUSC#\_STAGE POWER



<Variant Name>

<b>ASUS</b>		Title :POWER_LOAD SWITCH	
<OrigName>		Engineer: Eric_Ho	
Size	Project Name	F70SL	Rev 1.0
Custom			
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The schematic diagram illustrates the power management section of the TPC28T board. It shows the connection of various power pins (DDR\_PWRGD, SUS\_PWRGD, 1.5VS\_PWRGD, VCCP\_PWRGD, NV\_PWRGD\_VGA, VRM\_PWRGD) to the internal power regulation circuitry. Key components include the NC7SZ08P5X inverter (U9201), the 1SS355 Schottky diode (D9201), the UM6K1N MOSFETs (Q9201A, Q9201B), and the 4.7UF/6.3V MLCC capacitor (C9201). The circuit is powered by +3VO and +3VS rails. Signal pins T9201, T9202, T9203, T9204, and T9205 are also shown.

<Variant Name>		 <b>Title :</b> POWER_PROTECT	
<OrgName>		<b>Engineer:</b> Eric_Ho	
Size B	Project Name <b>F70SL</b>		Rev 1.0
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